MIDRANGE INPUT SYNCHRONOUS BUCK CONTROLLER WITH ADVANCED SEQUENCING AND OUTPUT MARGINING

FEATURES

- Operation over 4.5 V to 18 V Input Range
- 100 kHz to 1 MHz Voltage Mode Control
- Output Voltage Range From 0.69 V to 5.5 V
- Simultaneous, Ratiometric and Sequential Startup Sequencing
- Remote Sensing (Via Separate GND/PGND)
- 24-Pin QFN Package
- Thermal Shutdown
- Programmable Overcurrent Protection
- Power Good Indicator
- 1%, 690-mV Reference
- Output Margining, 3% and 5%
- Programmable UVLO and Hysteresis
- Frequency Synchronization

APPLICATIONS

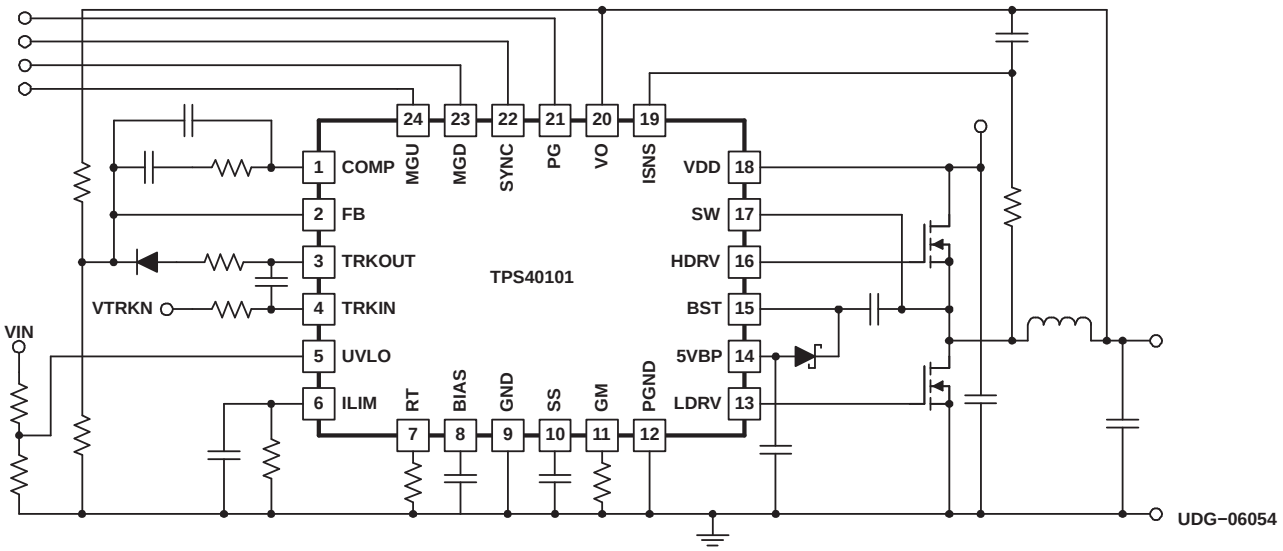
- Servers
- Networking Equipment
- Telecommunications Equipment
- Power Supply Modules

CONTENTS

DESCRIPTION

The TPS40101 is a wide-input synchronous, step-down controller that offers programmable closed loop soft-start, programmable UVLO and hysteresis, programmable current limit with hiccup recovery and can be synchronized to other timebases. The TPS40101 incorporates MOSFET gate drivers for external N-channel MOSFETs. Gate drive logic incorporates adaptive anti-cross conduction circuitry for improved efficiency, reducing diode conduction in the rectifier MOSFET.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER(1)
-40°C to 85°C	QFN	TPS40101RGER
		TPS40101RGET

(1) The QFN package (RGE) is available taped and reeled only. Use large reel device type R (TPS40101RGER) to order quantities of 3,000 per reel. Use small reel device type T (TPS40101RGET) to order quantities of 250 per reel.

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS40101	UNIT
V_{IN}	Input voltage range	VDD	-0.3 to 20	V
		5VBP, BIAS, FB, ILIM, ISNS, LDRV, MGU, MGD, PG, SS, SYNC, UVLO, VO	-0.3 to 6	
		BST to SW, HDRV to SW(2)	-0.3 to 6.0	
		SW	-1.5 to V_{VIN}	
		SW (transient) < 100 ns	-6 to 30	
		TRKIN	-0.3 to 20	
		GND to PGND	-0.3 to 0.3	
		TRKOUT	-0.3 to 8.0	
I_{IN}	Input current range	HDRV, LDRV (RMS)	0.5	A
		HDRV, LDRV (peak)	2.0	
		FB, COMP, TRKOUT	10 to -10	mA
		SS	20 to -20	mA
		PG	20	
		GM	1	
		RT	10	
		V5BP	50(3)	
		RT source	100	µA
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) BST to SW and HDRV to SW are relative measurements. BST and HDRV can be this amount of voltage above or below the voltage at SW.
(3) V5BP current includes gate drive current requirements. Observe maximum T_J rating for the device.

ELECTRICAL CHARACTERISTICS

-40°C ≤ T_A = T_J ≤ 85°C, V_{VDD} = 12 V, R_{RT} = 182 kΩ, R_{GM} = 232 kΩ, R_{ILIM} = 121 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{VDD}	Operating range		4.5		18.0	V
OPERATING CURRENT						
I_{DD}	Quiescent current	V_{FB} > 0.8 V, 0% duty cycle	1.3	1.8	2.5	mA
I_{SD}	Shutdown current	V_{UVLO} < 1 V		500		µA
5VPB						
	Internal regulator	7 V ≤ V_{VDD} ≤ 18 V, 0 mA ≤ I_{LOAD} ≤ 30 mA	4.7	5.0	5.3	V
		4.5 V ≤ V_{VDD} < 7 V, 0 mA ≤ I_{LOAD} ≤ 30 mA	4.3	5.0	5.3	
OSCILLATOR/RAMP GENERATOR						
f_{SW}	Programmable oscillator frequency		100		1000	kHz
f_{OSC}	Oscillator frequency accuracy	4.5 V ≤ V_{IN} < 18 V, -40°C ≤ T_A = T_J ≤ 125°C	250	275	300	
V_{RAMP}	Ramp amplitude(1)			0.5		V_{P-P}
t_{OFF}	Fixed off-time			100	150	ns
D_{MIN}	Minimum duty cycle				0%	
t_{MIN}	Minimum controllable pulse width(1)	C_{LOAD} = 4.7 nF, -40°C ≤ T_A = T_J ≤ 125°C		90	100	ns
V_{VLY}	Valley voltage(1)		1.0	1.6	2.0	V
FREQUENCY SYNCHRONIZATION						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	
I_{SYNC}	Input current, SYNC	V_{SYNC} = 2.5 V	4.0	5.5	10.0	µA
t_{SYNC}	Mimimum pulse width, SYNC		50			ns
t_{SYNC_SH}	Minimum set-up/hold time, SYNC(2)		100			
SOFT-START AND FAULT IDLE						
I_{SS}	Soft-start source (charge) current		13	20	25	µA
I_{SS_SINK}	Soft-start sink (discharge) current		3.4	5.0	6.6	
V_{SSC}	Soft-start completed voltage		3.25	3.40	3.75	V
V_{SSD}	Soft-start discharged voltage		0.15	0.20	0.25	
	Retry interval time to SS time ratio(1)		16			
V_{SSOS}	Offset from SS to error amplifier		300	500	800	mV
ERROR AMPLIFIER						
GBWP	Gain bandwidth product(1)		3.5	5.0		MHz
AVOL	Open loop		60	80		dB
I_{BIAS}	Input bias current, FB			50	200	nA
I_{OH}	High-level output current		2	3		mA
I_{OL}	Low-level output current		2	3		
	Slew rate(1)			2.1		V/µs
FEEDBACK REFERENCE						
V_{FB}	Feedback voltage reference	T_A = T_J = 25°C	686	690	694	mV
		-40°C < T_A = T_J ≤ 125°C	683		697	

(1) Ensured by design. Not production tested.
(2) To meet set up time requirements for the synchronization circuit, a negative logic pulse must be greater than 100 ns wide.

ELECTRICAL CHARACTERISTICS (continued)

-40°C ≤ T_A = T_J ≤ 85°C, V_{VDD} = 12 V, R_{RT} = 182 kΩ, R_{GM} = 232 kΩ, R_{ILIM} = 121 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE MARGINING						
V_{FBMGU}	Feedback voltage margin 5% up	V_{MGU} ≤ 500 mV	715	725	735	mV
	Feedback voltage margin 3% up	2 V ≤ V_{MGU} ≤ 3 V	700	711	720	
I_{MGUP}	Margin-up bias current		60	80	100	µA
V_{FBMGD}	Feedback voltage margin 5% down	V_{MGD} ≤ 500 mV	645	655	665	mA
	Feedback voltage margin 3% down	2 V ≤ V_{MGD} ≤ 3 V	660	669	680	
I_{MGDN}	Margin-down bias current		60	80	100	µA
t_{MGDLY}	Margining delay time(3)			12	30	ms
t_{MGTRAN}	Margining transition time		1.5	7.0		
CURRENT SENSE AMPLIFIER						
gm_{CSA}	Current sense amplifier gain	T_J =25°C	300	333	365	µS
TC_{GM}	Amplifier gain temperature coefficient			-2000		ppm/°C
V_{GMLIN}	Gm linear range voltage	T_J =25°C	-50		50	mV
I_{ISNS}	Bias current at ISNS pin	V_{VO} = V_{ISNS} = 3.3 V			250	nA
V_{GMCM}	Input voltage common mode		0		6	V
		4.5 V ≤ V_{IN} ≤ 5.5 V	0		3.6	
CURRENT LIMIT						
V_{ILIM}	ILIM pin voltage to trip overcurrent		1.44	1.48	1.52	V
$t_{ILIMDLY}$	Current limit comparator propagation delay	HDRV transition from on to off		70	140	ns
DRIVER SPECIFICATIONS						
t_{RHDRV}	HIgh-side driver rise time(4)	C_{LOAD} = 4.7 nF		57		ns
t_{FHDRV}	HIgh-side driver fall time(4)	C_{LOAD} = 4.7 nF		47		
$I_{HDRVSRPKS}$	HIgh-side driver peak source current(4)			800		mA
$I_{HDRVSRMIL}$	HIgh-side driver source current at 2.5 V(4)	V_{HDRV} - V_{SW} = 2.5 V		700		
$I_{HSDVSNPK}$	HIgh-side driver peak sink current(4)			1.3		A
$I_{HDRVSNMIL}$	High-side driver sink current at 2.5 V(4)	V_{HDRV} - V_{SW} = 2.5 V		1.2		
R_{HDRVUP}	HIgh-side driver pullup resistance	I_{HDRV} = 300 mA		2.4	4.0	Ω
R_{HDRVDN}	HIgh-side driver pulldown resistance	I_{HDRV} = 300 mA		1.0	1.8	
t_{RLDRV}	Low-side driver rise time(4)	C_{LOAD} = 4.7 nF		57		ns
t_{FLDRV}	Low-side driver fall time(4)	C_{LOAD} = 4.7 nF		47		
$I_{LDRVSRPK}$	Low-side driver peak source current(4)			800		mA
$I_{LDRVSNMIL}$	Low-side driver source current at 2.5 V(4)	V_{LDRV} = 2.5 V		700		
$I_{LSDVSNPK}$	Low-side driver peak sink current(4)			1.3		A
	Low-side driver sink current at 2.5 V(4)	V_{LDRV} = 2.5 V		1.2		
R_{LDRVUP}	Low-side driver pullup resistance	I_{LDRV} = 300 mA		2.0	4.0	Ω
R_{LDRVDN}	Low-side driver pulldown resistance	I_{LDRV} = 300 mA		0.8	1.5	
I_{SWLEAK}	Leakage current from SW pin		-1		1	µA
POWERGOOD						
V_{LPGD}	Powergood low voltage	I_{PGD}= 2 mA		30	100	mV
t_{PGD}	Powergood delay time		15	25	35	µs
V_{LPGDNP}	Powergood low voltage , no device power	V_{VDD} = OPEN, 10-kΩ pullup to external 5-V supply		1.00	1.25	V
V_{OV}	Power good overvoltage threshold, V_{FB}			765		mV
V_{UV}	Power good undervoltage threshold, V_{FB}			615		

(3) Margining delay time is the time delay from an assertion of a margining command until the output voltage begins to transition to the margined voltage.
(4) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

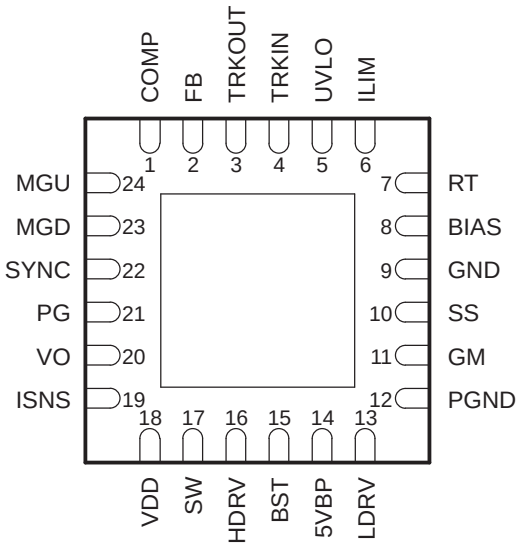
-40°C ≤ T_A = T_J ≤ 85°C, V_{VDD} = 12 V, R_{RT} = 182 kΩ, R_{GM} = 232 kΩ, R_{ILIM} = 121 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRACKING AMPLIFIER						
V_{TRKOS}	Tracking amplifier input offset voltage	V_{TRKOS} = V_{TRKIN} - V_O ; V_{VO} ≤ 2 V	7	25	40	mV
		V_{TRKOS} = V_{TRKIN} - V_O ; 2 V < V_{VO} ≤ 6 V	-5	25	40	
V_{TRKCM}	Input common mode, active range		0		6	V
V_{TRK}	Tracking amplifier voltage range	4.5 V ≤ V_{VDD} ≤ 5.5 V	0		3.6	
		5 V < V_{VDD} ≤ 18 V (5)	0		6	
$V_{HTRKOUT}$	High-level output voltage, TRKOUT	V_{VDD} = 12 V	5.0	6.5	8.0	
		V_{VDD} = 4.5 V	3.2	3.6		
$V_{LTRKOUT}$	Low-level output voltage, TRKOUT		0		0.5	
$I_{SRCTRKOUT}$	Source current, TRKOUT		0.65	2.00		mA
$I_{SNKTRKOUT}$	Sink current, TRKOUT		1	2		
V_{TRKDIF}	Differential voltage from TRKIN to VO				18	V
$GBWP_{TRK}$	Tracking amplifier gain bandwidth product (6)		1			MHz
$AVOL_{TRK}$	Tracking amplifier open loop DC gain (6)		60			dB
PROGRAMMABLE UVLO						
V_{UVLO}	Undervoltage lockout threshold		1.285	1.332	1.378	V
I_{UVLO}	Hysteresis current		9.0	10.0	10.8	µA
INTERNALLY FIXED UVLO						
$V_{UVLOFON}$	Fixed UVLO turn-on voltage at VDD pin	-40°C ≤ T_A < 125°C	3.850	4.150	4.425	V
$V_{UVLOFOFF}$	Fixed UVLO turn-off voltage at VDD pin		3.750	4.06	4.35	
$V_{UVLOHYST}$	UVLO hysteresis at VDD pin			85		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature (6)		130	165		°C
T_{SDHYST}	Hysteresis (6)			25		

(5) Amplifier can track to the lesser of 6 V or (V_{DD} × 0.95)
(6) Ensured by design. Not production tested.

DEVICE INFORMATION

RGE PACKAGE
(BOTTOM VIEW)

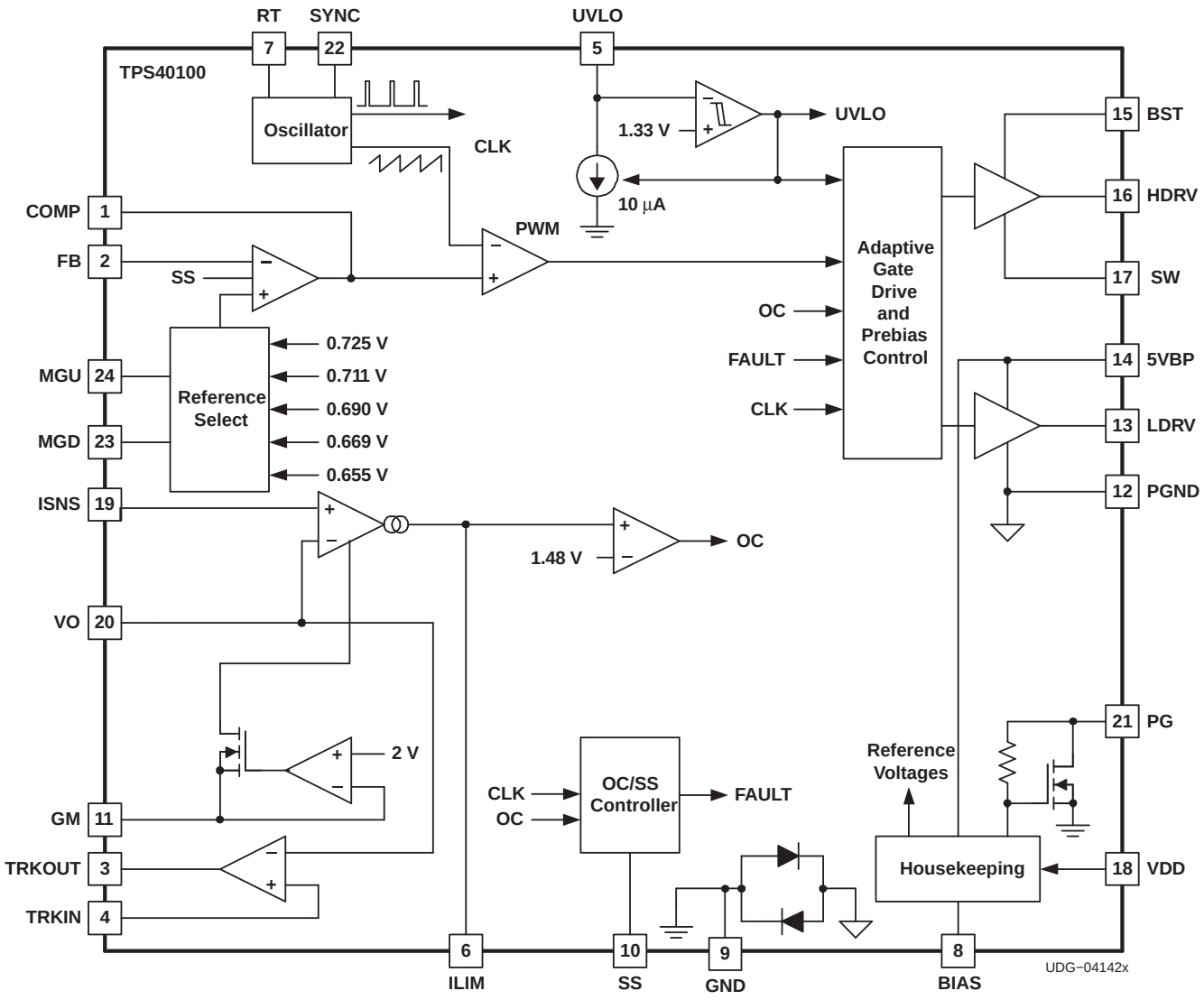


DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
5VBP	14	O	Output of an internal 5-V regulator. A 1-µF bypass capacitor should be connected from this pin to PGND. Power for external circuitry may be drawn from this pin. The total gate drive current and external current draw should not cause the device to exceed thermal capabilities
BIAS	8	O	The bypassed supply for internal device circuitry. Connect a 0.1-µF or greater ceramic capacitor from this pin to GND.
BST	15	I	Gate drive voltage for the high-side N-channel MOSFET. An external diode must be connected from 5VBP (A) to BST(K). A schottky diode is recommended for this purpose. A capacitor must be connected from this pin to the SW pin.
COMP	1	O	Output of the error amplifier. A feedback network is connected from this pin to the FB pin for control loop compensation.
FB	2	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage (approximately 690 mV).
GM	11	I	Connect a resistor from this pin to GND to set the gain of the current sense amplifier.
GND	9	-	Low power or signal ground for the device. All *signal* level circuits should be referenced to this pin unless otherwise noted.
HDRV	16	O	Floating gate drive for the high side N-channel MOSFET.
ILIM	6	O	Current limit pin used to set the overcurrent threshold and transient ride out time. An internal current source that is proportional to the inductor current sets a voltage on a resistor connected from this pin to GND. When this voltage reaches 1.48 V, an overcurrent condition is declared by the device. Adding a capacitor in parallel with the resistor to GND sets a time delay that can be used to help avoid nuisance trips.
ISNS	19	I	Current input from the inductor DCR sensing. This input signal is one of the inputs of the current sense amplifier for over current detection.
LDRV	13	O	Gate drive for the N-channel synchronous rectifier.
MGD	23	I	Margin down pin used for load stress test. When this pin is pulled to GND through less than 10 kΩ, the output voltage is decreased by 5%. The 3% margin down at the output voltage is accommodated when this pin is connected to GND through a 30-kΩ resistor.
MGU	24	I	Margin up pin used for load stress test. When this pin is pulled to GND through less than 10 kΩ, the output voltage is increased by 5%. The 3% margin up at the output voltage is accommodated when this pin is connected to GND through a 30-kΩ resistor.
PG	21	O	Open drain power good output for the device. This pin is pulled low when the voltage at the FB pin is more than 10% higher or lower than 690 mV, a UVLO condition exists, soft-start is active, tracking is active, an overcurrent condition exists or the die is over temperature.
PGND	12	-	Power ground for internal drivers
RT	7	I	A resistor connected from this pin to GND sets operating frequency.
SS	10	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. This pin is also used as a time out function during an overcurrent event.
SW	17	I	Connected to the switched node of the converter. This pin is the return line for the flying high side driver.
SYNC	22	I	Rising edge triggered synchronization input for the device. This pin can be used to synchronize the oscillator frequency to an external master clock. This pin may be left floating or grounded if the function is not used.
TRKIN	4	I	Control input allowing simultaneous startup of multiple controllers. The converter output tracks TRKIN voltage with a small controlled offset (typically 25 mV) when the tracking amplifier is used. See application secttion for more information.
TRKOUT	3	O	Output of the tracking amplifier. If the tracking feature is used, this pin should be connected to FB pin through a resistor in series with a diode. The resistor value can be calculated from the equivalent impedance at the FB node. The diode should be a low leakage type to minimize errors due to diode reverse current. For further information on compensation of the tracking amplifier refer to the application information
UVLO	5	I	Provides for programming the undervoltage lockout level and serves as a shutdown input for the device.
VDD	18	I	Supply voltage for the device.
VO	20	I	Output voltage. This is the reference input to the current sense amplifier.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE (NO SWITCHING)

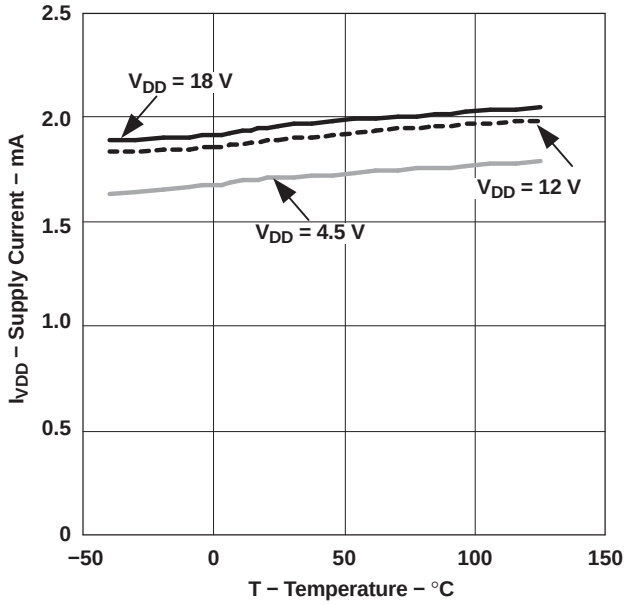


Figure 1.

SHUTDOWN SUPPLY CURRENT vs TEMPERATURE

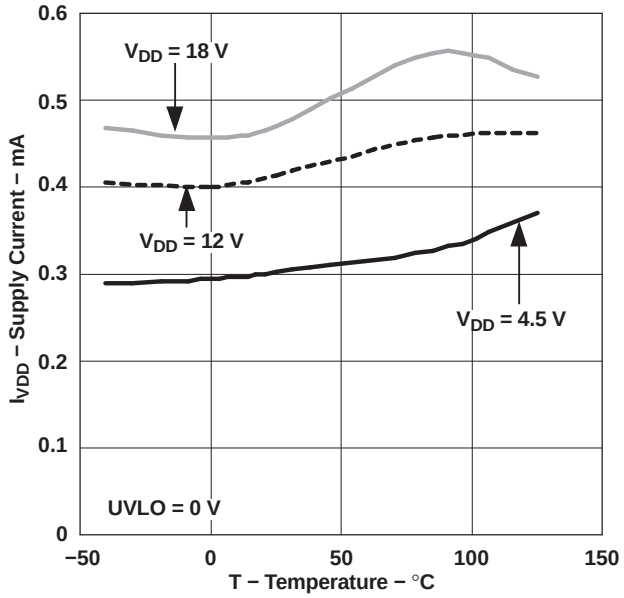


Figure 2.

REGULATOR OUTPUT VOLTAGE vs TEMPERATURE

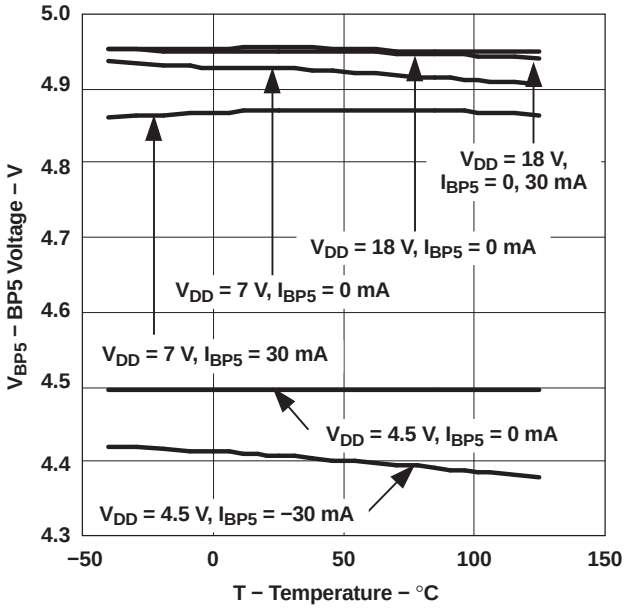


Figure 3.

FEEDBACK BIAS CURRENT vs TEMPERATURE

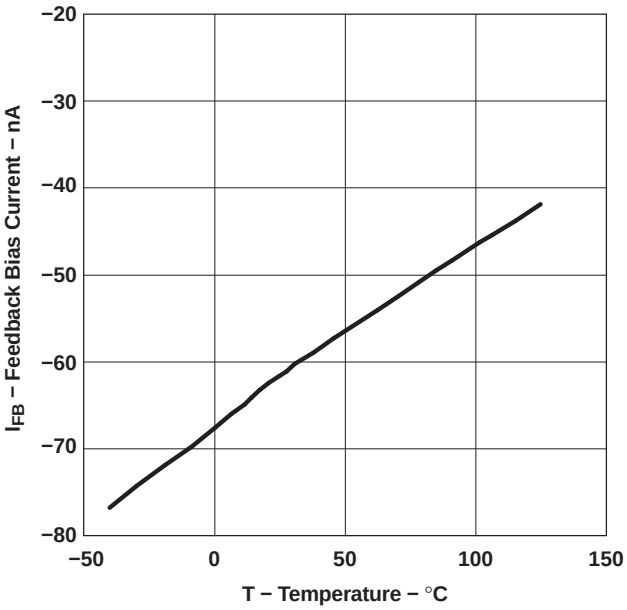


Figure 4.

TYPICAL CHARACTERISTICS (continued)

REFERENCE VOLTAGE CHANGE
vs
TEMPERATURE

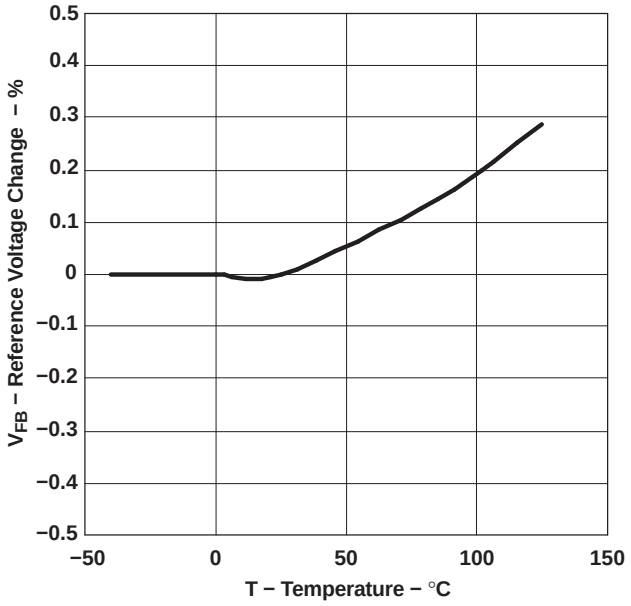


Figure 5.

MARGIN DELAY
vs
TEMPERATURE

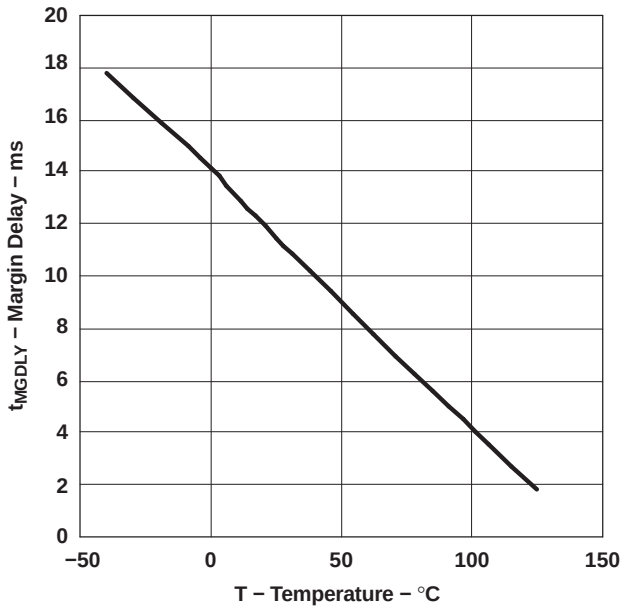


Figure 6.

MARGIN TRANSITION
vs
TEMPERATURE

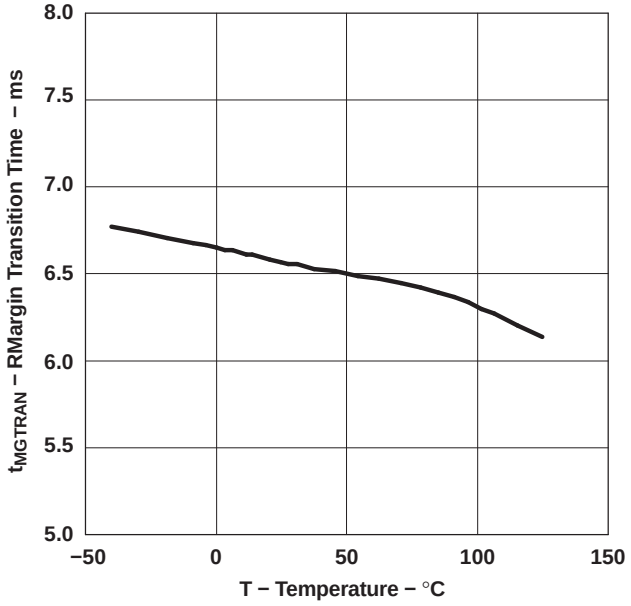


Figure 7.

POWERGOOD UNDERVOLTAGE THRESHOLD
vs
TEMPERATURE

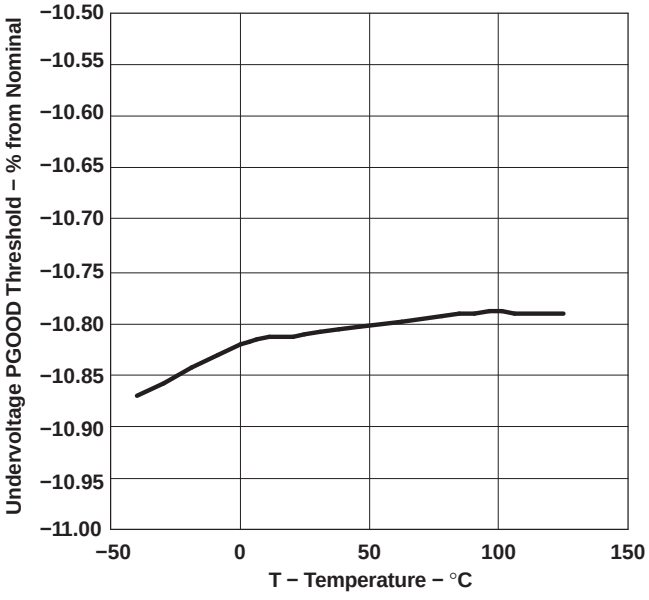


Figure 8.

TYPICAL CHARACTERISTICS (continued)

POWERGOOD OVERVOLTAGE THRESHOLD vs TEMPERATURE

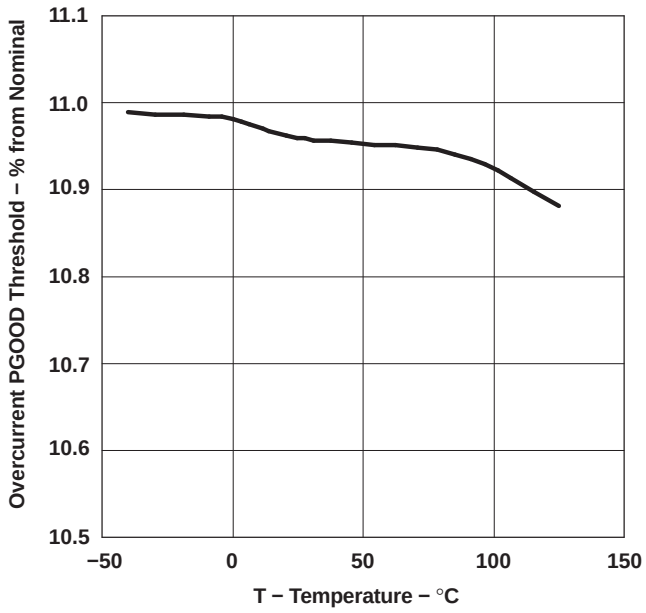


Figure 9.

FIXED UVLO VOLTAGE vs TEMPERATURE

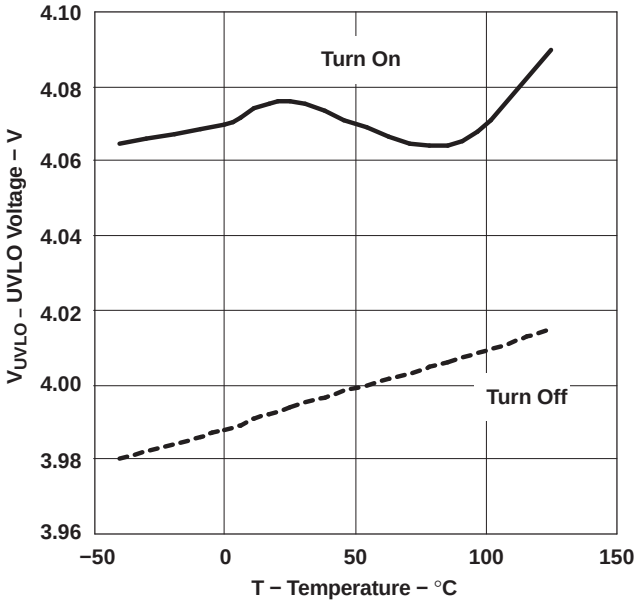


Figure 10.

PROGRAMMABLE UVLO THRESHOLD vs TEMPERATURE

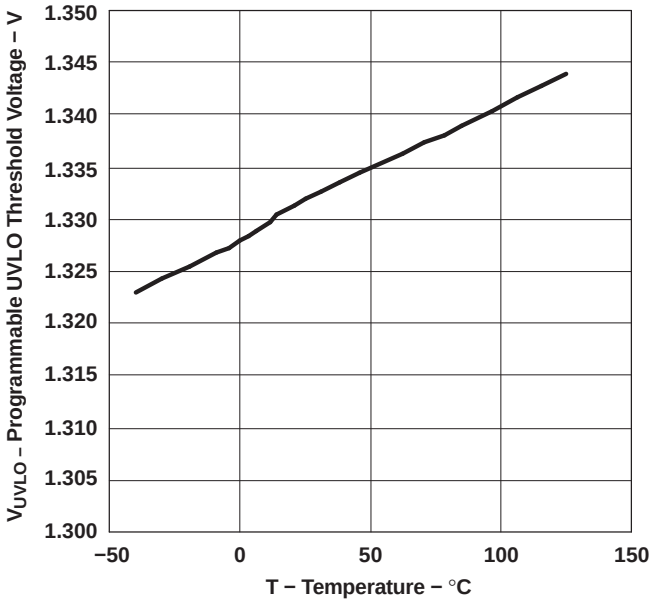


Figure 11.

PROGRAMMABLE UVLO HYSTERESIS CURRENT vs TEMPERATURE

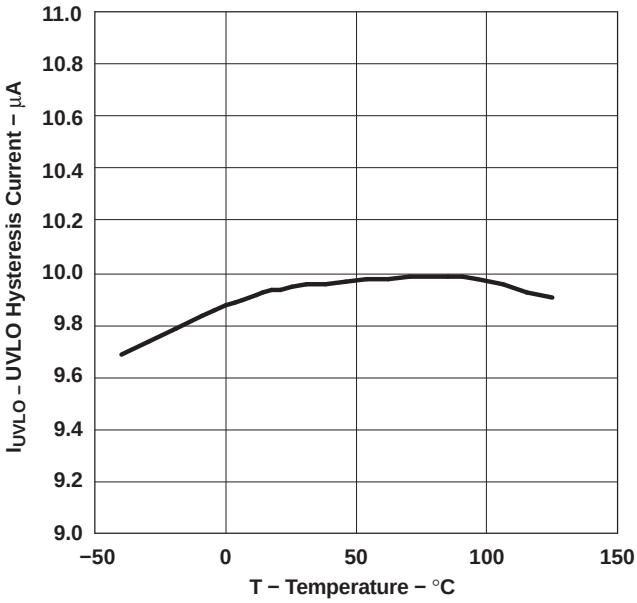


Figure 12.

TYPICAL CHARACTERISTICS (continued)

FREQUENCY CHANGE
vs
TEMPERATURE

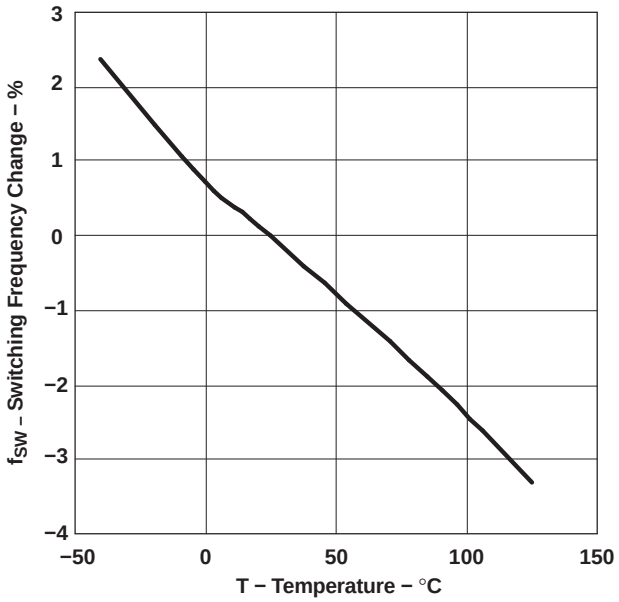


Figure 13.

TRACKING AMPLIFIER OFFSET VOLTAGE
vs
TEMPERATURE

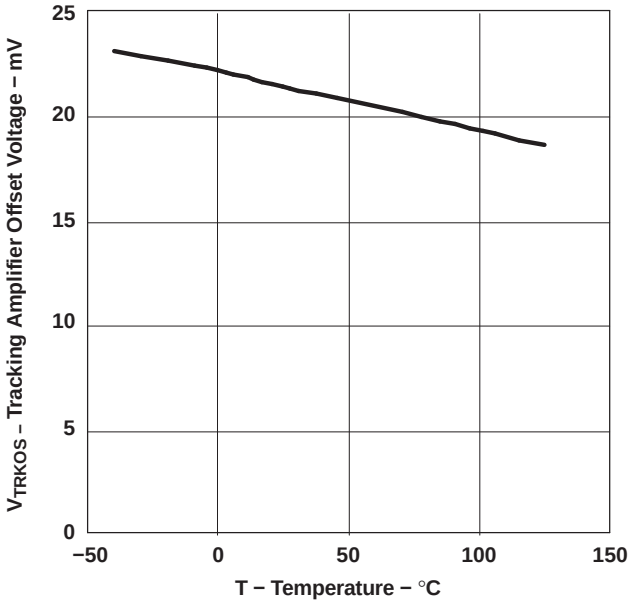


Figure 14.

TRACKING AMPLIFIER OUTPUT VOLTAGE
vs
TEMPERATURE

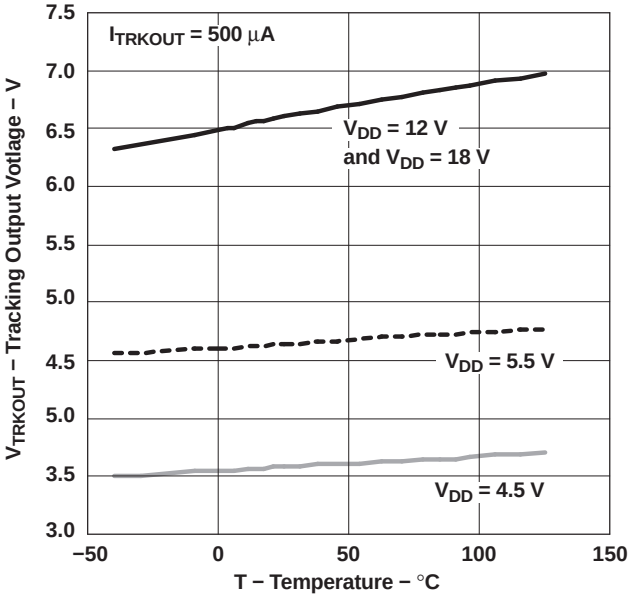


Figure 15.

TRACKING AMPLIFIER BIAS CURRENT
vs
TEMPERATURE

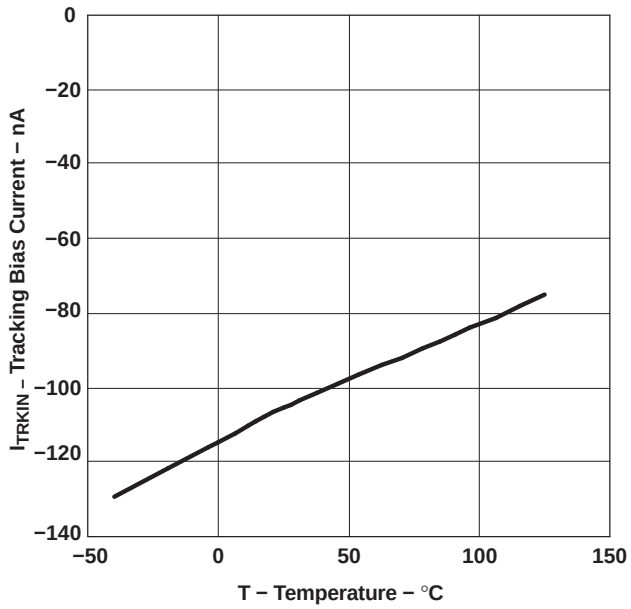


Figure 16.

TYPICAL CHARACTERISTICS (continued)

SOFT-START CHARGE AND DISCHARGE vs TEMPERATURE

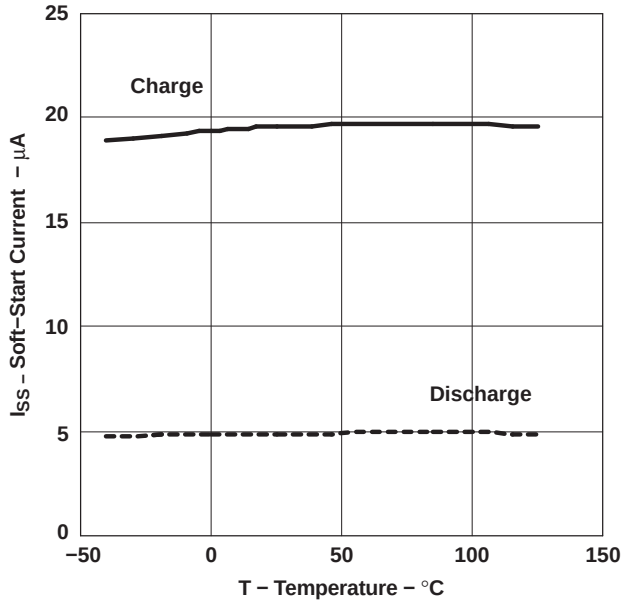


Figure 17.

POWER GOOD VOLTAGE vs TEMPERATURE

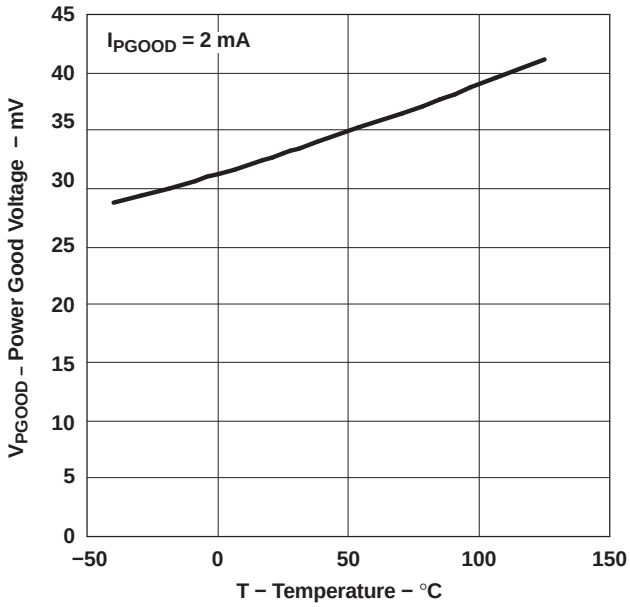


Figure 18.

CURRENT LIMIT THRESHOLD VOLTAGE vs TEMPERATURE

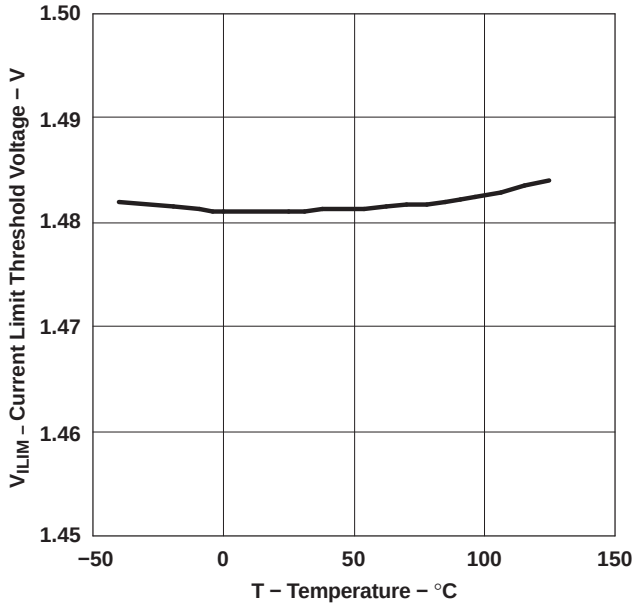


Figure 19.

OUTPUT VOLTAGE BIAS CURRENT vs TEMPERATURE

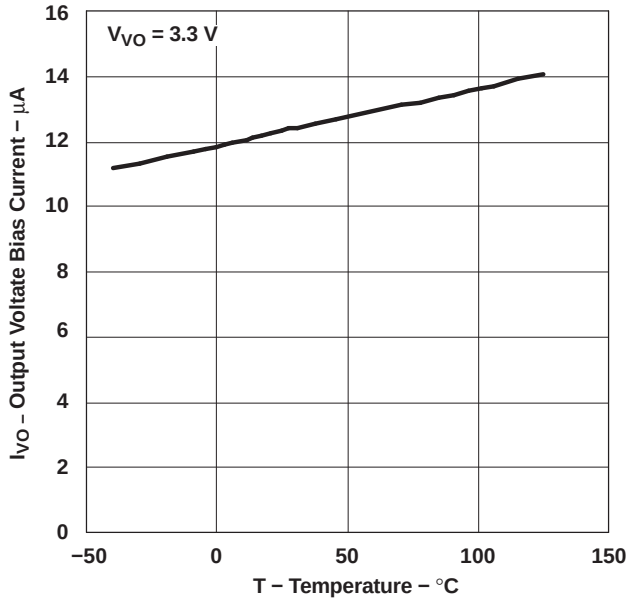


Figure 20.

TYPICAL CHARACTERISTICS (continued)

CURRENT SENSE BIAS CURRENT vs TEMPERATURE

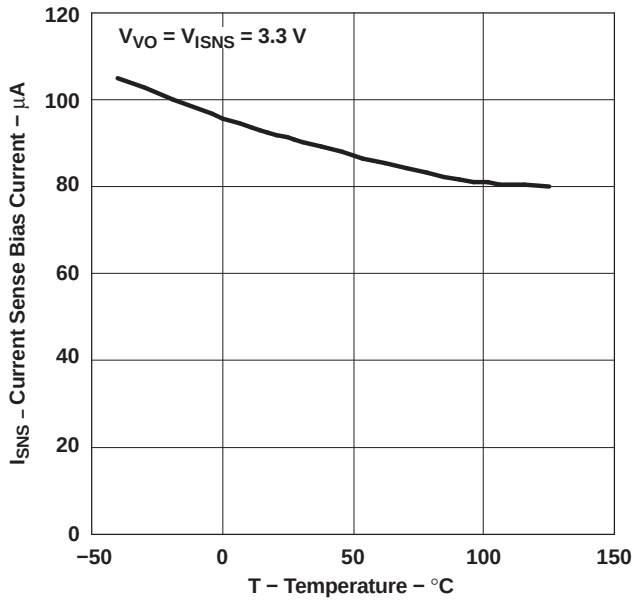


Figure 21.

CURRENT SENSE BIAS CURRENT vs CURRENT SENSE VOLTAGE

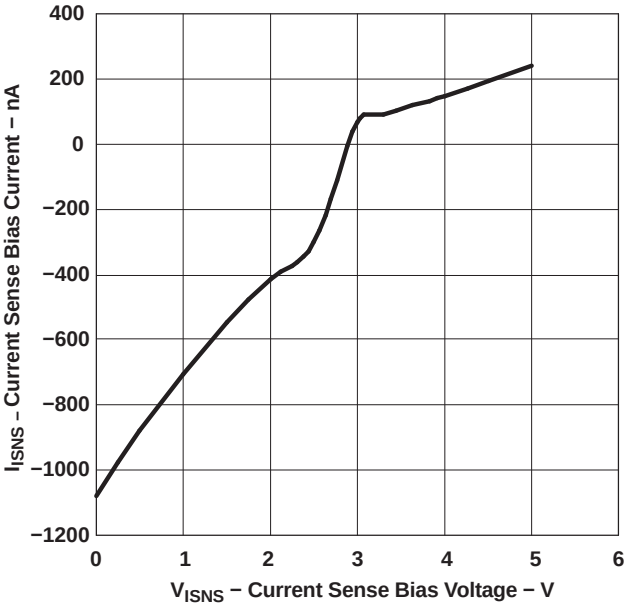


Figure 22.

CURRENT SENSE BIAS CURRENT vs TEMPERATURE

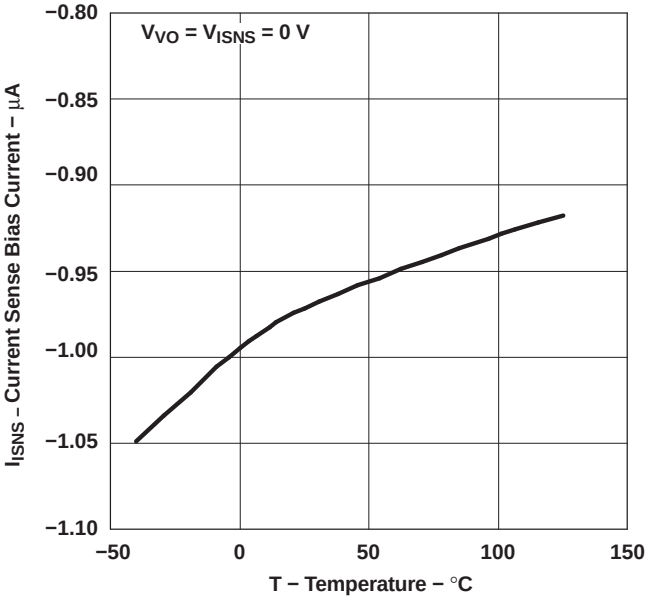


Figure 23.

RELATIVE CURRENT SENSE AMPLIFIER GAIN vs TEMPERATURE

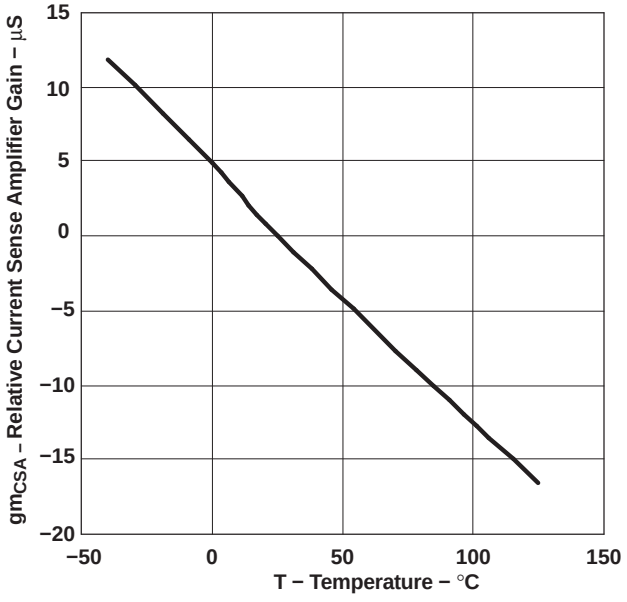


Figure 24.

TYPICAL CHARACTERISTICS (continued)

TIMING RESISTOR
vs
SWITCHING FREQUENCY
(100 kHz to 400 kHz)

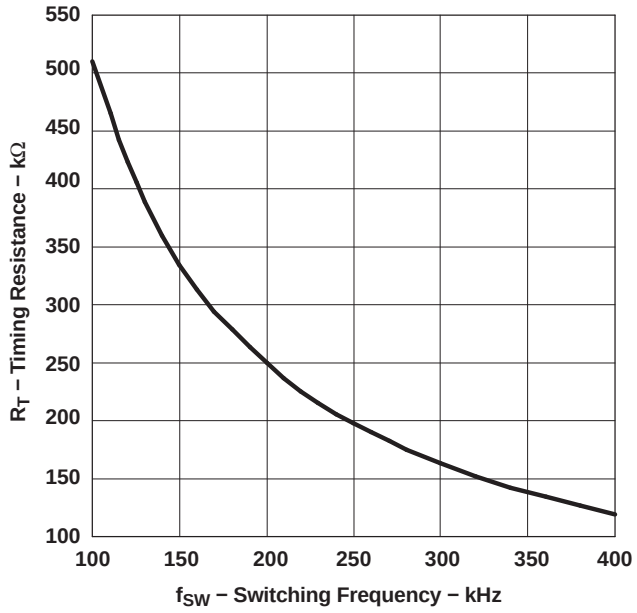


Figure 25.

TIMING RESISTOR
vs
SWITCHING FREQUENCY
(400 kHz to 1 MHz)

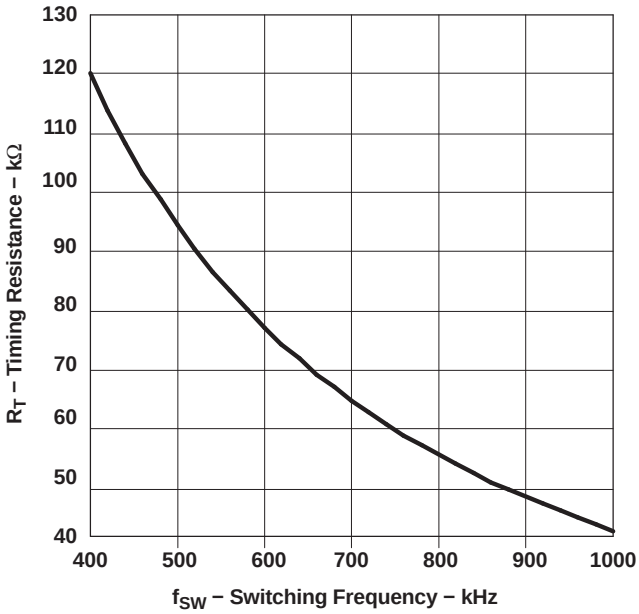


Figure 26.

CURRENT SENSE AMPLIFIER GAIN SETTING
RESISTANCE
vs
CURRENT SENSE AMPLIFIER GAIN
R_{GM} > 50 kΩ

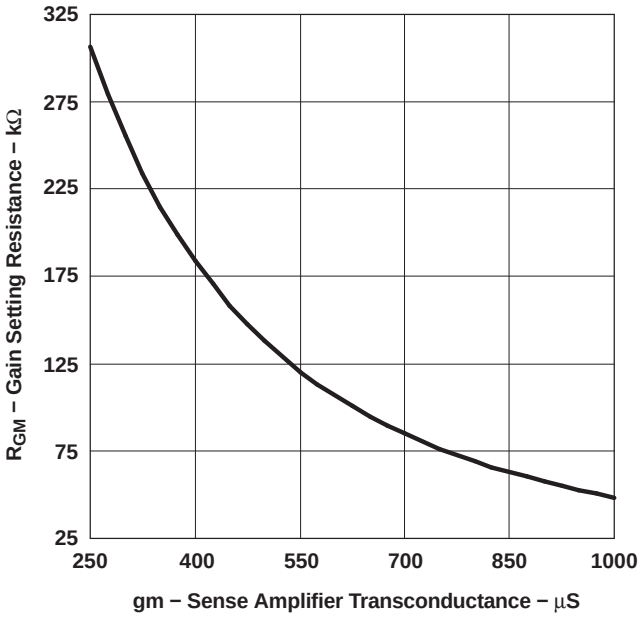


Figure 27.

POWERGOOD VOLTAGE
vs
POWERGOOD CURRENT (NO DEVICE POWER)

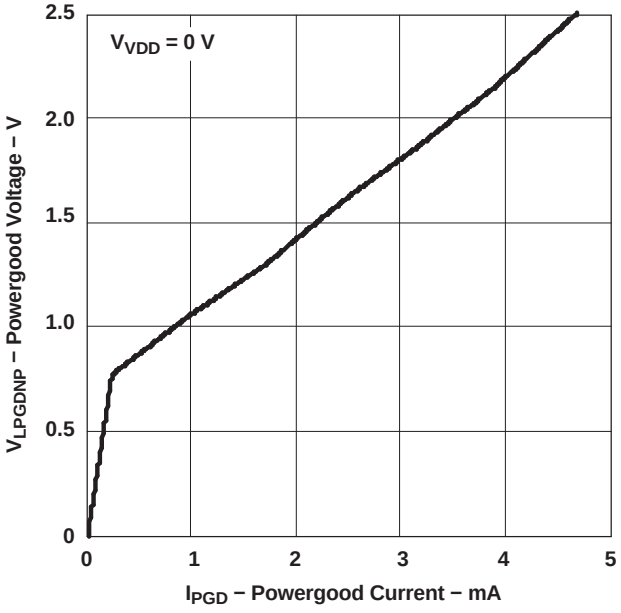


Figure 28.

APPLICATION INFORMATION

Introduction

The TPS40101 is a voltage mode synchronous buck controller targeted at applications that require sequencing and output voltage margining features.Current sensing is true differential and can be done using the inductor DC resistance (with a R-C filter) or with a separate sense resistor in series with the inductor. The programmable overcurrent function has user programmable integration to eliminate nuisance tripping and allow the user to tailor the response to application requirements. The controller provides an integrated method to margin the output voltage to ±3% and ±5% of its nominal value by simply grounding one of two pins directly or through a resistance. Powergood and clock synchronization functions are provided on dedicated pins. Users can program operating frequency and the closed loop soft-start time by means of a resistor and capacitor to ground respectively. Output sequencing/tracking can be accomplished in one of three ways: sequential (one output comes up, then a second comes up), ratiometric (one or more outputs reach regulation at the same time – the voltages all follow a constant ratio while starting) and simultaneous (one or more outputs track together on startup and reach regulation in order from lowest to highest).

Programming Operating Frequency

Operating frequency is set by connecting a resistor to GND from the RT pin. The relationship is:

$$R_T = \left[\frac{-3.98 \times 10^4}{f_{SW}^{\ 2}}\right] + \left(\frac{5.14 \times 10^4}{f_{SW}}\right) - 8.6\ (k\Omega) \quad (1)$$

where

- f_{SW} is the switching frequency in kHz
- R_T is in kΩ

Figure 25 and Figure 26 show the relationship between the switching frequency and the R_T resistor as described in Equation 1. The scaling is different between them to allow the user a more accurate views at both high and low frequency.

Selecting an Inductor Value

The inductor value determines the ripple current in the output capacitors and has an effect on the achievable transient response. A large inductance decreases ripple current and output voltage ripple, but is physically larger than a smaller inductance at the same current rating and limits output current slew rate more that a smaller inductance would. A lower inductance increases ripple current and output voltage ripple, but is physically smaller than a larger inductance at the same current rating. For most applications, a good compromise is selecting an inductance value that gives a ripple current between 20% and 30% of the full load current of the converter. The required inductance for a given ripple current can be found from:

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN} \times f_{SW} \times \Delta I} \quad (H) \quad (2)$$

where

- L is the inductance value (H)
- V_{IN} is the input voltage to the converter (V)
- V_{OUT} is the output voltage of the converter (V)
- f_{SW} is the switching frequency chosen for the converter (Hz)
- ΔI is the peak-to-peak ripple current in the inductor (A)

Selecting the Output Capacitance

The required value for the output capacitance depends on the output ripple voltage requirements and the ripple current in the inductor, as well as any load transient specifications that may exist.

The output voltage ripple depends directly on the ripple current and is affected by two parameters from the output capacitor: total capacitance and the capacitors equivalent series resistance (ESR). The output ripple voltage (worst case) can be found from:

APPLICATION INFORMATION (continued)

$$\Delta V = \Delta I \times \left[ESR + \left(\frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \right] \quad (V) \tag{3}$$

where

- ΔV is the peak to peak output ripple voltage (V)
- ΔI is the peak-to-peak ripple current in the inductor (A)
- f_{SW} is the switching frequency chosen for the converter (Hz)
- C_{OUT} is the capacitance value of the output capacitor (F)
- ESR is the equivalent series resistance of the capacitor, C_{OUT} (Ω)

For electrolytic capacitors, the output ripple voltage is almost entirely (90% or more) due to the ESR of the capacitor. When using ceramic output capacitors, the output ripple contribution from ESR is much smaller and the capacitance value itself becomes more significant. Paralleling output capacitors to achieve a desired output capacitance generally lowers the effective ESR more effectively than using a single larger capacitor. This increases performance at the expense of board area.

If there are load transient requirements that must be met, the overshoot and undershoot of the output voltage must be considered. If the load suddenly increases, the output voltage momentarily dips until the current in the inductor can ramp up to match the new load requirement. If the feedback loop is designed aggressively, this undershoot can be minimized. For a given undershoot specification, the required output capacitance can be found by:

$$C_{O(under)} = \frac{L \times I_{STEP}^{2}}{2 \times V_{UNDER} \times D_{MAX} \times \left(V_{IN} - V_{OUT} \right)} \quad (F) \tag{4}$$

where

- $C_{O(under)}$ is the output capacitance required to meet the undershoot specification (F)
- L is the inductor value (H)
- I_{STEP} is the change in load current (A)
- V_{UNDER} is the maximum allowable output voltage undershoot
- D_{MAX} is the maximum duty cycle for the converter
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Similarly, if the load current suddenly goes from a high value to a low value, the output voltage overshoots. The ouput voltage rises until the current in the inductor drops to the new load current. The required capacitance for a given amount of overshoot can be found by:

$$C_{O(over)} = \frac{L \times I_{STEP}^{2}}{2 \times V_{OVER} \times V_{OUT}} \quad (F) \tag{5}$$

where

- $C_{O(over)}$ is the output capacitance required to meet the undershoot specification (F)
- L in the inductor value (H)
- I_{STEP} is the change in load current (A)
- V_{OVER} is the maximum allowable output voltage overshoot
- V_{OUT} is the output voltage

The required value of output capacitance is the maximum of $C_{O(under)}$ and $C_{O(over)}$.

Knowing the inductor ripple current, the switching frequency, the required load step and the allowable output voltage excursion allows calculation of the required output capacitance from a transient response perspective. The actual value and type of output capacitance is the one that satisfies both the ripple and transient specifications.

APPLICATION INFORMATION (continued)

Calculating the Current Sense Filter Network

The TPS40101 gets current feedback information by sensing the voltage across the inductor resistance, R_{LDC}. In order to do this, a filter must be constructed that allows the sensed voltage to be representative of the actual current in the inductor. This filter is a series R-C network connected across the inductor as shown in Figure 29.

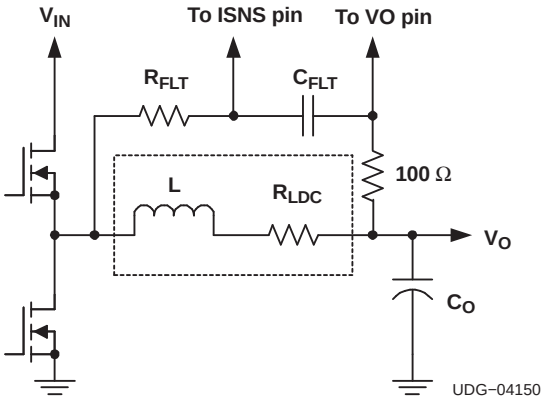


Figure 29. Current Sensing Filter Circuit

If the R_{FLT}-C_{FLT} time constant is matched to the L/R_{LDC} time constant, the voltage across C_{FLT} is equal to the voltage across R_{LDC}. It is recommended to keep R_{FLT} 10 kΩ or less. C_{FLT} can be arbitrarily chosen to meet this condition (100 nF is suggested). R_{FLT} can then be calculated.

$$R_{FLT} = \frac{L}{R_{LDC} \times C_{FLT}} - 100 \ (\Omega) \tag{6}$$

where

- R_{FLT} is the current sense filter resistance (Ω)
- C_{FLT} is the current sense filter capacitance (F)
- L is the output inductance (H)
- R_{LDC} is the DC resistance of the output inductor (Ω)

When laying out the board, better performance can be accomplished by locating C_{FLT} as close as possible to the VO and ISNS pins. The closer the two resistors can be brought to the device the better as this reduces the length of high impedance runs that are susceptible to noise pickup. The 100-Ω resistor from V_{OUT} to the VO pin of the device is to limit current in the event that the output voltage dips below ground when a short is applied to the output of the converter.

Compensation for Inductor Resistance Change Over Temperature

The resistance in the inductor that is sensed is the resistance of the copper winding. This value changes over temperature and has approximately a 4000 ppm/°C temperature coefficient. The gain of current sense amplifier in the TPS40101 has a built in temperature coefficient of approximately -2000 ppm/°C. If the circuit is physically arranged so that there is good thermal coupling between the inductor and the device, the thermal shifts tend to offset. If the thermal coupling is perfect, the net temperature coefficient is 2000 ppm/°C. If the coupling is not perfect, the net temperature coefficient lies between 2000 ppm/°C and 4000 ppm/°C. For most applications this is sufficient. If desired, the temperature drifts can be compensated for. The following compensation scheme assumes that the temperature rise at the device is directly proportional to the temperature rise at the inductor. If this is not the case, compensation accuracy suffers. Also, there is generally a time lag in the temperature rise at the device vs. at the inductor that could introduce transient errors beyond those predicted by the compensation.

Also, the 100-Ω resistor in Figure 29 is not shown. However, it is required if the output voltage can dip below ground during fault conditions. The calculations are not afffected, other than increasing the effective value of R_{F1} by 100-Ω.

APPLICATION INFORMATION (continued)

The relative resistance change in the inductor is given by:

$$R_{REL(L)} = 1 + TC_L \times \left(T_L - T_{BASE}\right) \quad \text{(dimensionless)} \tag{7}$$

where

- $R_{REL(L)}$ is the relative resistance of the inductor at T_L compared to the resistance at T_{BASE}
- TC_L is the temperature coefficient of copper, 4000 ppm/°C or 0.004
- T_L is the inductor copper temperature (°C)
- T_{BASE} is the reference temperature, typically lowest ambient (°C)

The relative gain of the current sense amplifier is given by a similar equation:

$$gm_{(REL)} = 1 + TC_{GM} \times \left(T_{IC} - T_{BASE}\right) \quad \text{(dimensionless)} \tag{8}$$

where

- $gm_{(REL)}$ is the relative gain of the amplifier at T_{IC} compared to the gain at T_{BASE}
- TC_{GM} is the temperature coefficient of the amplifier gain, -2000 ppm/°C or -0.002
- T_{IC} is the device junction temperature (°C)
- T_{BASE} is the reference temperature, typically lowest ambient (°C)

The temperature rise of the device can usually be related to the temperature rise of the inductor. The relationship between the two temperature rises can be approximated as a linear relationship in most cases:

$$T_{IC} - T_{BASE} = \left(T_L - T_{BASE}\right) \times k_{THM} \tag{9}$$

where

- T_{IC} is the device junction temperature (°C)
- T_{BASE} is the reference temperature, typically lowest ambient (°C)
- T_L is the inductor copper temperature (°C)
- k_{THM} is the constant that relates device temperature rise to the inductor temperature rise and must be determined experimentally for any given design

With these assumptions, the effective inductor resistance over temperature is:

$$R_{REL(eff)} = R_{REL(L)} \times gm_{REL} = \left[1 + TC_L\left(T_L - T_{BASE}\right)\right] \times \left[1 + k_{THM} \times TC_{GM} \times \left(T_L - T_{BASE}\right)\right] \quad \text{(dimensionless)} \tag{10}$$

$R_{REL(eff)}$ is the relative effective resistance that must be compensated for when doing the compensation. The circuit of Figure 30 shows a method of compensating for thermal shifts in current limit. The NTC thermistor (R_{NTC}) must be well coupled to the inductor. C_{FLT} should be located as close to the device as possible.

APPLICATION INFORMATION (continued)

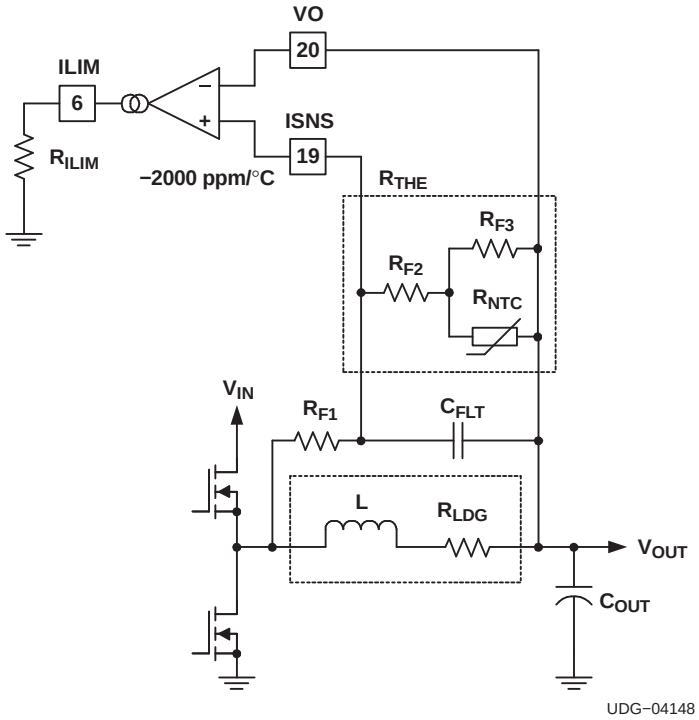


Figure 30. Compensation for Temperature Coefficient of the Inductor Resistance

The first step is to determine an attenuation ratio α. This ratio should be near to 1 but not too close. If it is too close to 1, the circuit requires large impedances and thermistor values too high. If α is too low, the current signal is attenuated unnecessarily. A suggested value is 0.8.

$$\alpha \cong 0.8 \frac{R_{THE}}{R_{THE} + R_{F1}} \text{ (dimensionless)} \tag{11}$$

R_{THE} is the equivalent resistance of the R_{F2}-R_{F3}-R_{NTC} network:

$$R_{THE} = R_{F2} + \frac{R_{F3} \times R_{NTC}}{R_{F3} + R_{NTC}} \ (\Omega) \tag{12}$$

The base temperature (T_{BASE}) should be selected to be the lowest temperature of interest for the thermal matching – the lowest ambient expected. The resistance of the inductor at this base temperature should be used to calculate effective resistance. The expected current sense amplifier gain at T_{BASE} should be used for calculating over current components (R_{ILIM}).

The next step is to decide at what two temperatures the compensation is matched to the response of the deviceand inductor copper, T1 and T2. Once these are chosen, an NTC thermistor can be chosen and its value found from its data sheet at these two temperatures: $R_{NTC(T1)}$ and $R_{NTC(T2)}$. The component values in the network can be calculated using the following equations:

APPLICATION INFORMATION (continued)

$$R_{F1} = \frac{L}{R_{LDC(Tbase)} \times C_{FLT} \times \alpha} \quad (\Omega) \tag{13}$$

$$R_{LDC(T1)} = R_{LDC(Tbase)} \times R_{REL(effT1)} \quad (\Omega) \tag{14}$$

$$R_{LDC(T2)} = R_{LDC(Tbase)} \times R_{REL(effT2)} \quad (\Omega) \tag{15}$$

$$R_{THE(T1)} = \frac{\alpha \times R_{LDC(Tbase)} \times R_{F1}}{R_{LDC(T1)} - \alpha \times R_{LDC(Tbase)}} \quad (\Omega) \tag{16}$$

$$R_{THE(T2)} = \frac{\alpha \times R_{LDC(Tbase)} \times R_{F1}}{R_{LDC(T2)} - \alpha \times R_{LDC(Tbase)}} \quad (\Omega) \tag{17}$$

$$a = 1 - \frac{R_{NTC(T1)} - R_{NTC(T2)}}{R_{THE(T1)} - R_{THE(T2)}} \quad \text{(dimensionless)} \tag{18}$$

$$b = R_{NTC(T1)} + R_{NTC(T2)} \quad (\Omega) \tag{19}$$

$$c = R_{NTC(T1)} \times R_{NTC(T2)} \quad (\Omega^2) \tag{20}$$

$$R_{F3} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (\Omega) \tag{21}$$

$$R_{F2} = \frac{R_{THE(T1)} \times \left(R_{F3} + R_{NTC(T1)}\right) - R_{F3} \times R_{NTC(T1)}}{R_{F3} + R_{NTC(T1)}} \quad (\Omega) \tag{22}$$

where

- L is the value of the output inductance (H)
- C_{FLT} is the value of the current sense filter capacitor (F)
- α is the attenuation ratio chosen from Equation 11
- $R_{THE(T1)}$, $R_{THE(T2)}$ are the equivalent resistances of the R_{THE} network at temperatures T1 and T2
- $R_{LDC(Tbase)}$ is the DC resistance of the inductor at temperature T_{BASE} in Ω
- $R_{LDC(T1)}$, $R_{LDC(T2)}$ are the inductor resistances at temperatures T1 and T2
- $R_{REL(effT1)}$, $R_{REL(effT2)}$, are the relative resistances of the inductor at T1 and T2 vs. Tbase
- $R_{NCT(T1)}$, $R_{NTC(T2)}$ are the effective resistance of the NTC thermistor at temperatures T1 and T2

Setting the Current Sense Amplifier Gain

The amplifier is a transconductance type and its gain is a set by connecting a resistor from the GM pin to GND:

$$R_{GM} = \frac{3}{43.443 \times gm_{CSA}{}^2 + 0.01543 \times gm_{CSA} + 3.225 \times 10^{-6}} \quad (\Omega) \tag{23}$$

where

- R_{GM} is the resistor that sets the gain of the amplifier (Ω)
- gm_{CSA} is the gain of the current sense amplifier (S)

The value of the sense amplifier gain should be less than 1000 µS, and more than 250 µS, with the resulting gain setting resistor greater than 50 kΩ. As a suggested starting point, set the gain of the current sense amplifier to a nominal 400 µS with R_{GM} of 182 kΩ. This value should accommodate most applications adequately. Figure 27 shows the current sense amplifier gain setting resistance vs. the sense amplifier gain.

APPLICATION INFORMATION (continued)

Establishing Tracking and Designing a Tracking Control Loop

The tracking startup feature of the TPS40101 is a separate control loop that controls the output voltage to a reference applied to the TRKIN pin. This reference voltage is typically a ramp generated by an external R-C circuit. Connecting the junction of R5, C5 and R6 (see Figure 31) of multiple converters together allows the converters output voltages to track together during start up. A controlled power down is accomplished by pulling down the common junction in a controlled manner and then removing power to the converters or turning them off by grounding the UVLO pin.The relevant circuit fragment is shown in Figure 31.

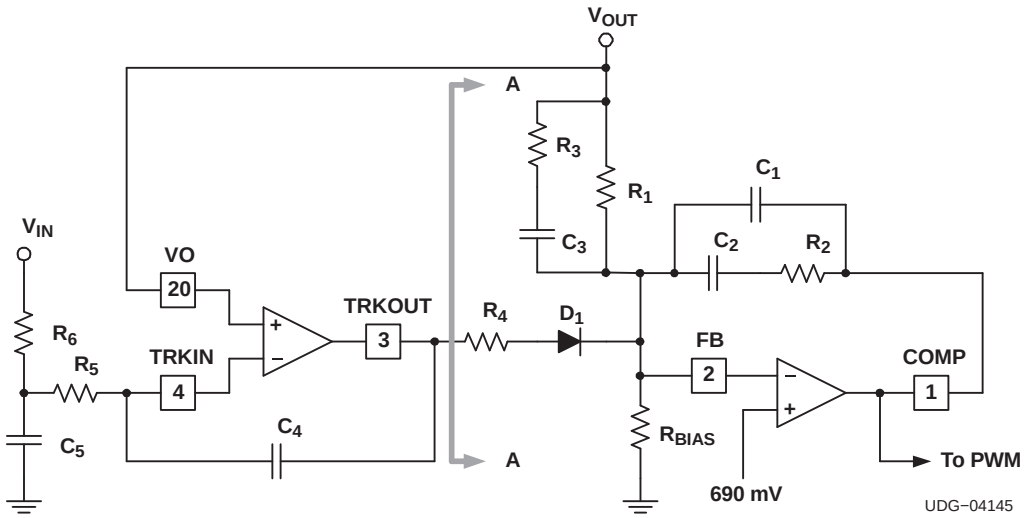


Figure 31. Tracking Loop Control Schematic

First, select a value for R_4. In order for this circuit to work properly, the output of the tracking amplifier must be able to cause the FB pin to reach at least 690 mV with the output voltage at zero volts. This is so that the output voltage can be forced to zero by the tracking amplifier. This places a maximum value on R_4:

$$R_4 < \frac{\left[V_{HTRKOUT(min)} - V_{DIODE} - V_{FB}\right]}{V_{FB}} \times \frac{R_1 \times R_{BIAS}}{R_1 + R_{BIAS}} \ \Omega \tag{24}$$

where

- $V_{HTRKOUT(min)}$ is the minimum output voltage of the tracking amplifier (see Electrical Characteristics table)
- V_{DIODE} is the forward voltage of the device selected for D_1
- V_{FB} is the value of the reference voltage (690 mV)

R_4 should not be chosen much lower than this value since that unnecessarily increases tracking loop gain, making compensation more difficult and opening the door to potential non-linear control issues. D1 could be a schottky if the impedance of the R_1-R_{BIAS} string is low enough that the leakage current is not a consequence. Be aware that schottky diode leakage currents rise significantly at elevated temperature. If elevated temperature operation and increased accuracy are important, use a standard or low leakage junction diode or the base-emitter junction of a transistor for D_1.

Once R_4 is selected, the gain of the closed loop power supply looking into “A” is known. That gain is the ratio of R_1 and R_4:

$$\frac{dV_{OUT}}{dV_{TRKOUT}} = -\frac{R_1}{R_4} \text{ (dimensionless)} \tag{25}$$

The tracking loop itself should have a crossover frequency much less that the crossover frequency of the voltage control loop. Typically, the tracking loop crossover frequency is 1/10th or less of the voltage loop crossover frequency to avoid loop interactions. Note that the presence of the diode in the circuit gives a non-linear control mechanism for the tracking loop. The presence of this non-linearity makes designing a control loop more challenging. The simplest approach is to simply limit the bandwidth of this loop to no more than necessary.

APPLICATION INFORMATION (continued)

Knowing the gain of the voltage loop looking into R_4 and the desired tracking loop crossover frequency, R_5 and C_4 can be found:

$$R_5 \times C_4 = \frac{R_4}{2\pi \times R_1 \times f_{cTRK}} \quad (s) \tag{26}$$

where

- f_{CTRK} is the desired tracking loop crossover frequency

The actual values of R_5 and C_4 are a balance between impedance level and component size. Any of a range of values is applicable. In general, R_5 should be no more than 20% of R_6, and less than 10 kΩ. If this is done, then R_6 can safely be ignored for purposes of tracking loop gain calculations. For general usage, R_6 should probably be between 100 kΩ and 500 kΩ.

If an overshoot bump is present on the output at the beginning a tracking controlled startup, the tracking loop bandwidth is likely too high. Reducing the bandwidth helps reduce the initial overshoot. See Figure 32 and Figure 33.

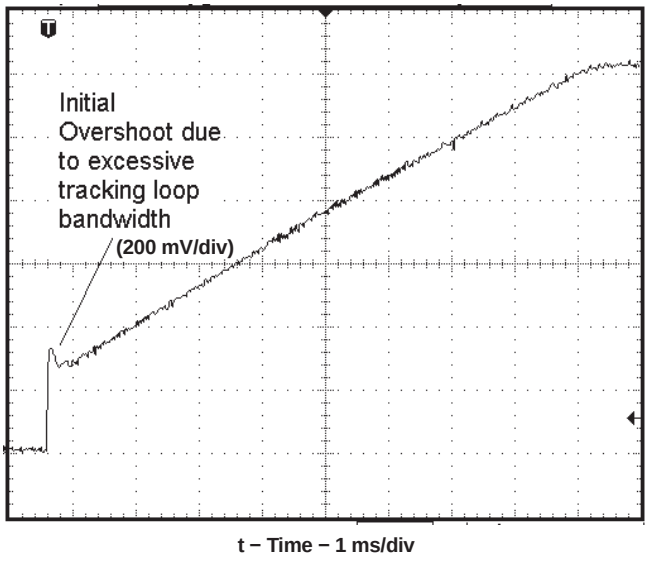


Figure 32. Excessive Tracking Loop Bandwidth

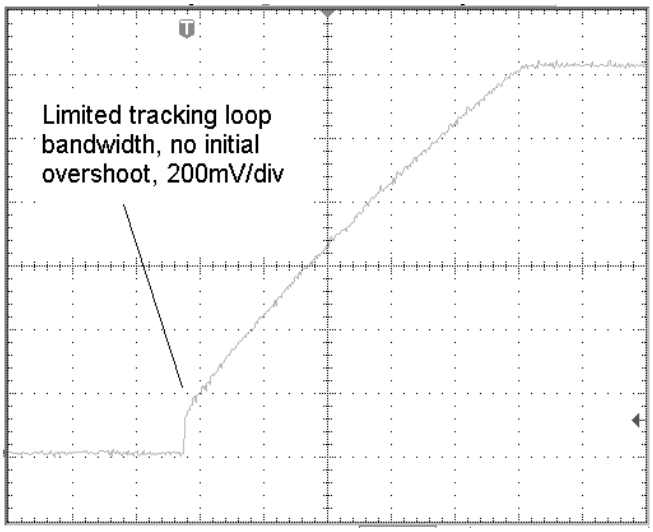


Figure 33. Limited Tracking Loop Bandwidth

The tracking ramp time is the time required for C_5 to charge to the same voltage as the output voltage of the converter.

$$t_{TRK} = -R_6 \times C_5 \times \ln\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (s) \tag{27}$$

where

- V_{OUT} is the output voltage of the converter
- V_{IN} is the voltage applied to the top of R_6
- t_{TRK} is the desired tracking ramp time

With these equations, it is possible to design the tracking loop so that the impedance level of the loop and the component size are balanced for the particular application. Note that higher impedances make the loop more susceptible to noise issues while lower impedances require increased capacitor size.

Figure 34 shows the spice model for the voltage loop expanded for use with the tracking loop.

APPLICATION INFORMATION (continued)

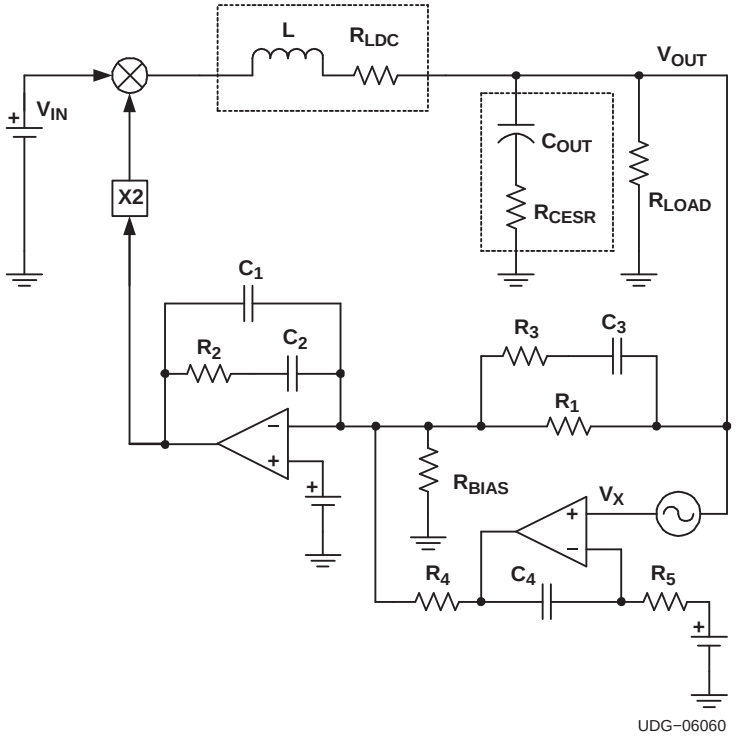


Figure 34. AC Behavioral Model for Tracking Control Loop

To use the model, the AC voltage source is swept over the frequency range of interest. The open loop ac response is V_X/V_{OUT}.

Programming Soft-Start Time

The soft-start time of the TPS40101 is fully user programmable by selecting a single capacitor. The SS pin sources 20 µA to charge this capacitor. The actual output ramp-up time is the amount of time that it takes for the 20 µA to charge the capacitor through a 690 mV range. There is some initial lag due to an offset from the actual SS pin voltage to the voltage applied to the error amplifier. See Figure 36. The soft-start is done in a closed loop fashion, meaning that the error amplifier controls the output voltage at all times during the soft start period and the feedback loop is never open as occurs in duty cycle limit soft-start schemes. The error amplifier has two non-inverting inputs, one connected to the 690 mV reference voltage, and one connected to the offset SS pin voltage. The lower of these two voltages is what the error amplifier controls the FB pin to. As the voltage on the SS pin ramps up past approximately 1.04 V (resulting in 690 mV at the error amplifier "+" input – See Figure 36), the 690 mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = T_{SS} \times \frac{20\ \mu A}{V_{FB}}\ F \tag{28}$$

where

- T_{SS} is the desired soft-start ramp time (s)
- C_{SS} is the required capacitance on the SS pin (F)
- V_{FB} is the reference voltage feedback loop (690 mV)

APPLICATION INFORMATION (continued)

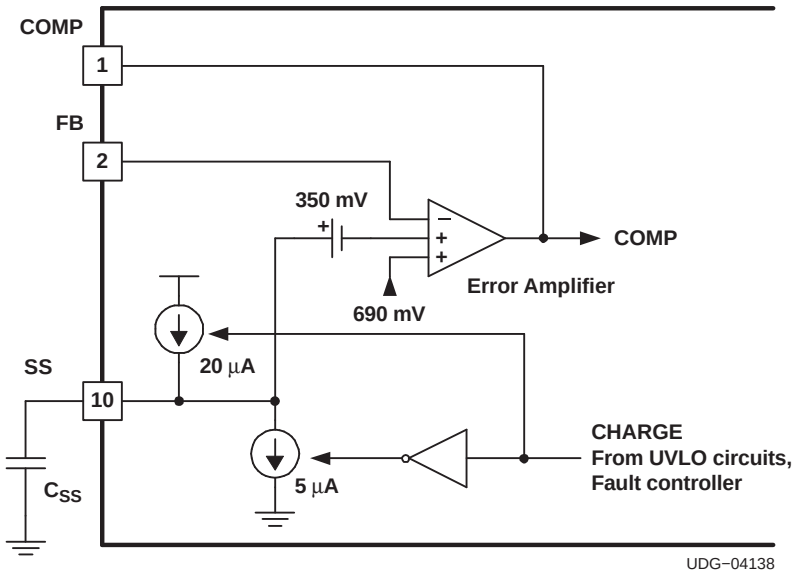


Figure 35. Error Amplifier and Soft-Start Functional Diagram

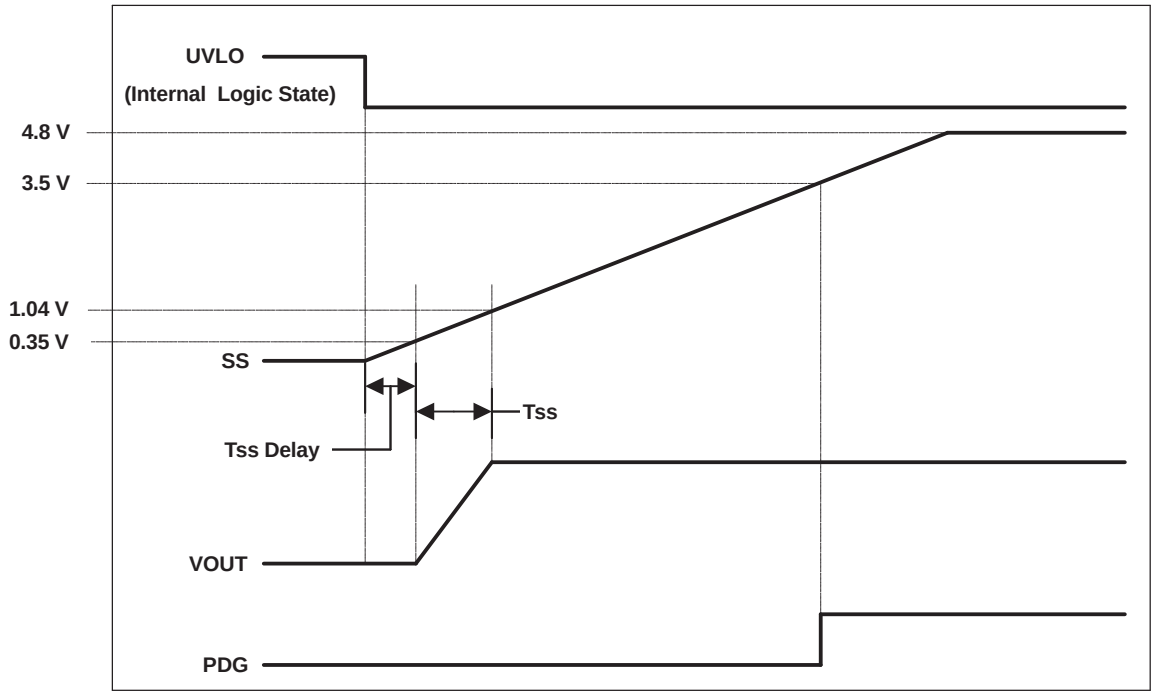


Figure 36. Relationship Between UVLO (Internal Logic State), SS, VOUT and PGD at Startup

APPLICATION INFORMATION (continued)

Interaction Between Soft-Start and Tracking Startup

Since the TPS40101 provides two means of controlling the startup (closed loop soft-start and tracking) care must be taken to ensure that the two methods do not interfere with each other. The two methods should not be allowed to try and control the output at the same time. If tracking is to be used, the reference input to the tracking amplifier (TRKIN) should be held low until soft-start completes, or the voltage at the SS pin is at least above 1.04 V. This ensures that the soft-start circuit is not trying to control the startup at the same time as tracking circuit. If it is desired to have soft-start control the startup, then there are two options:

- Disconnect the tracking amplifier output from the FB node (this is the recommended solution. The tracking amplifier can then be used for other system purposes if desired)
- Maintain the tracking amplifier output connection to the FB circuit - the reference to the tracking amplifier should be tied to VDD pin in this case. This places the tracking amplifier output (TRKOUT) in a low state continuously and therefore removes any influence the tracking circuit has on the converter startup.

Additionally, when tracking is allowed to control the startup, soft-start should not be set to an arbitrarily short time. This causes the output voltage to bump up when power is applied to the converter as soft-start ramps up quickly and the tracking loop (which is necessarily low bandwidth) cannot respond fast enough to control the output to zero voltage. In other words, the soft start ramp rate must be within the capability of the tracking loop to override.

Overcurrent Protection

Overcurrent characteristics are determined by connecting a parallel R-C network from the ILIM pin to GND. The ILIM pin sources a current that is proportional to the current sense amplifier transconductance and the voltage between ISNS and VO. This current produces a voltage on the R-C network at ILIM. If the voltage at the ILIM pin reaches 1.48 V, an overcurrent condition is declared and the outputs stop switching for a period of time. This time period is determined by the time is takes to discharge the soft-start capacitor with a controlled current sink. To set the overcurrent level:

$$R_{ILIM} = \frac{V_{ILIM}}{gm_{CSA} \times R_{LDC} \times I_{OC}} \ \Omega \tag{29}$$

where

- V_{ILIM} is the overcurrent comparator threshold (1.48 V typically)
- I_{OC} is the overcurrent level to be set
- gm_{CSA} is the transconductance of the current sensing amplifier
- R_{LDC} is the equivalent series resistance of the inductor (or the sense resistor value)
- R_{ILIM} is the value of the resistor from ILIM to GND

The response time of the overcurrent circuit is determined by the R-C time constant at the ILIM pin and the level of the overcurrent. The response time is given by:

$$t_{OC} = -R_{ILIM} \times C_{ILIM} \times \ln\left(1 - \frac{1}{n}\right) \ (s) \tag{30}$$

where

- t_{OC} is the response time before declaring an overcurrent
- R_{ILIM} (Ω) and C_{ILIM} (F) are the components connected to the ILIM pin
- n is the multiplier of the overcurrent. If the overcurrent is 2 times the programmed level, then n is 2.

By suitable manipulation of the time constant at ILIM, the overcurrent response can be tailored to ride out short term transients and still provide protection for overloads and short circuits. The gm of the current sense amplifier has a temperature coefficient of approximately -2000 ppm/°C. This is to help offset the temperature coefficient of resistance of the copper in the inductor, about +4000 ppm/°C. The net is a +2000 ppm/°C temperature coefficient. So, for a 100°C increase in temperature, the overcurrent threshold decreases by 20%, assuming good thermal coupling between the controller and the inductor. Temperature compensation can be done as described earlier if desired.

When an overcurrent condition is declared, the controller stops switching and turns off both the high-side

APPLICATION INFORMATION (continued)

MOSFET and the low-side MOSFET. The soft-start capacitor is then discharged at 25% of the charge rate during an overcurrent condition and the converter remains idle until the soft start pin reaches 200 mV, at which point the soft-start circuit starts charging again and the converter attempts to restart. In normal operation, the soft-start capacitor is charged to approximately 3.5 V when an initial fault is applied to the output. This means that the minimum time before the first restart attempt is:

$$t_{RESTART} = \frac{3.3 \times C_{SS}}{I_{SSDIS}} \quad (s) \tag{31}$$

where

- $t_{RESTART}$ is the initial restart time (s)
- C_{SS} is soft start capacitance (F)
- I_{SSDIS} is the soft start discharge current – 5 μA

If the output fault is persistent, and an overcurrent is declared on the restart, both of the MOSFETs are turned off and the soft-start capacitor continues to charge to 3.5 V and then discharge to 200 mV before another restart is attempted.

UVLO Programming

The TPS40101 provides the user with programmable UVLO level and programmable hysteresis. The UVLO detection circuit schematic is described in Figure 37 from a functional perspective.

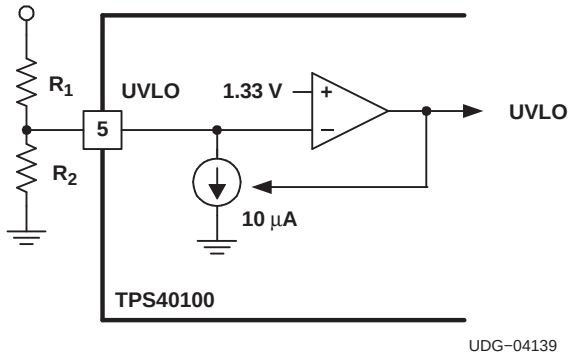


Figure 37. UVLO Circuit Functional Diagram

To program this circuit, first select the amount of hysteresis (the difference between the startup voltage and the shutdown voltage) desired:

$$R_1 = \frac{V_{HYST}}{I_{UVLO}} \ \Omega \tag{32}$$

Then select the turn-on voltage and solve for R_2.

$$R_2 = \frac{V_{UVLO} \times R_1}{V_{ON} - V_{UVLO} - R_1 \times I_{UVLO}} \ \Omega \tag{33}$$

where

- V_{HYST} is the desired level of hysteresis in the programmable UVLO circuit
- I_{UVLO} is the undervoltage lockout circuit hysteresis current (10 μA typ)
- V_{UVLO} is the UVLO comparator threshold voltage (1.33 V typ)

APPLICATION INFORMATION (continued)

Voltage Margining

The TPS40101 allows the user to make the output voltage temporarily be 3% above or below the nominal output, or 5% above or below the nominal output. This is accomplished by connecting the MGU or MGD pins to GND directly or through a resistance. See Table 1.

Table 1. Output Voltage Margining States

RESISTANCE TO GND (kΩ)		OUTPUT VOLTAGE
R_{MGU}	R_{MGD}	
OPEN	OPEN	Nominal
< 10	OPEN	+ 5%
OPEN	< 10	-5%
25 to 37	OPEN	+3%
OPEN	25 to 37	-3%

There are some important considerations when adjusting the output voltage.

- Only one of these pins should be anything other than an open circuit at any given time. States not listed in the table are invalid states and the behavior of the circuit may be erratic if this is tried.
- When changing the output voltage using the margin pins, it is very important to let the margin transition complete before altering the state of the margin pins again.
- Do not use mechanical means (switches, non-wetted relay contacts, etc) to alter the margining state. The contact bounce causes erratic behavior.

Synchronization

The TPS40101 may be synchronized to an external clock source that is faster than the free running frequency of the circuit. The SYNC pin is a rising edge sensitive trigger to the oscillator that causes the current cycle to terminate and starts the next switching cycle. It is recommended that the synchronization frequency be no more than 120% of the free running frequency. Following this guideline leads to fewer noise and jitter problems with the pulse width modulator in the device. The circuit can be synchronized to higher multiples of the free running frequency, but be aware that this results in a proportional decrease in the amplitude of the ramp from the oscillator applied to the PWM, leading to increased noise sensitivity and increased PWM gain, possibly affecting control loop stability.

The pulse applied to the SYNC pin can be any duty ratio as long as the pulse either high or low is at least 100 ns wide. Levels are logic compatible with any voltage under 0.8 V considered a *low* and any voltage over 2 V considered a *high*.

Power Good Indication

The PGD pin is an open drain output that actively pulls to GND if any of the following conditions are met (assuming that the input voltage is above 4.5V)

- Soft-start is active (V_{SS} < 3.5 V)
- Tracking is active (V_{TRKOUT} > 0.7 V)
- V_{FB} < 0.61 V
- V_{FB} > 0.77 V
- V_{UVLO} < 1.33 V
- Overcurrent condition exists
- Die temperature is greater than 165°C

A short filter (20 μs) must be overcome before PGD pulls to GND from a high state to allow for short transient conditions and noise and not indicate a power NOT good condition.

The PGD pin attempts to pull low in the absence of input power. If the VDD pin is open circuited, the voltage on PGD typically behaves as shown in Figure 28.

Pre-Bias Operation

Some applications require that the converter not sink current during startup if a pre-existing voltage exists at the output. Since synchronous buck converters inherently sink current some method of overcoming this characteristic must be employed. Applications that require this operation are typically power rails for a multiple supply processor or ASIC. The method used in this controller, is to not allow the low side or rectifier FET to turn on until the output voltage commanded by the start up ramp is higher than the pre-existing output voltage. This is detected by monitoring the internal pulse width modulator (PWM) for its first output pulse. Since this controller uses a closed loop startup, the first output pulse from the PWM does not occur until the output voltage is commanded to be higher than the pre-existing voltage. This effectively limits the controller to sourcing current only during the startup sequence. If the pre-existing voltage is higher that the intended regulation point for the output of the converter, the converter starts and sinks current when the soft-start time has completed.

Remote Sense

The TPS 40100 is capable of remotely sensing the load voltage to improve load regulation. This is accomplished by connecting the GND pin of the device and the feedback voltage divider as near to the load as possible.

CAUTION:

Trace Length Considerations

More than a few inches of trace length between the GND pin of the device and the load GND can lead to significantly increased pulse width jitter. As a starting point, the GND pin connection should be no further than six inches from the PGND connection. The actual distance that starts causing erratic behavior is application and layout dependent and must be evaluated on an individual basis. If the controller exhibits output pulse jitter in excess of 25 ns and the GND pin is tied to the load ground, connecting the GND pin closer to the PGND pin (and thereby sacrificing some load regulation) may improve performance. In either case, connecting the feedback voltage divider at the point of load should not cause any problems. For layout, the voltage divider components should be close to the device and a trace can be run from there to the load point.

Design Examples

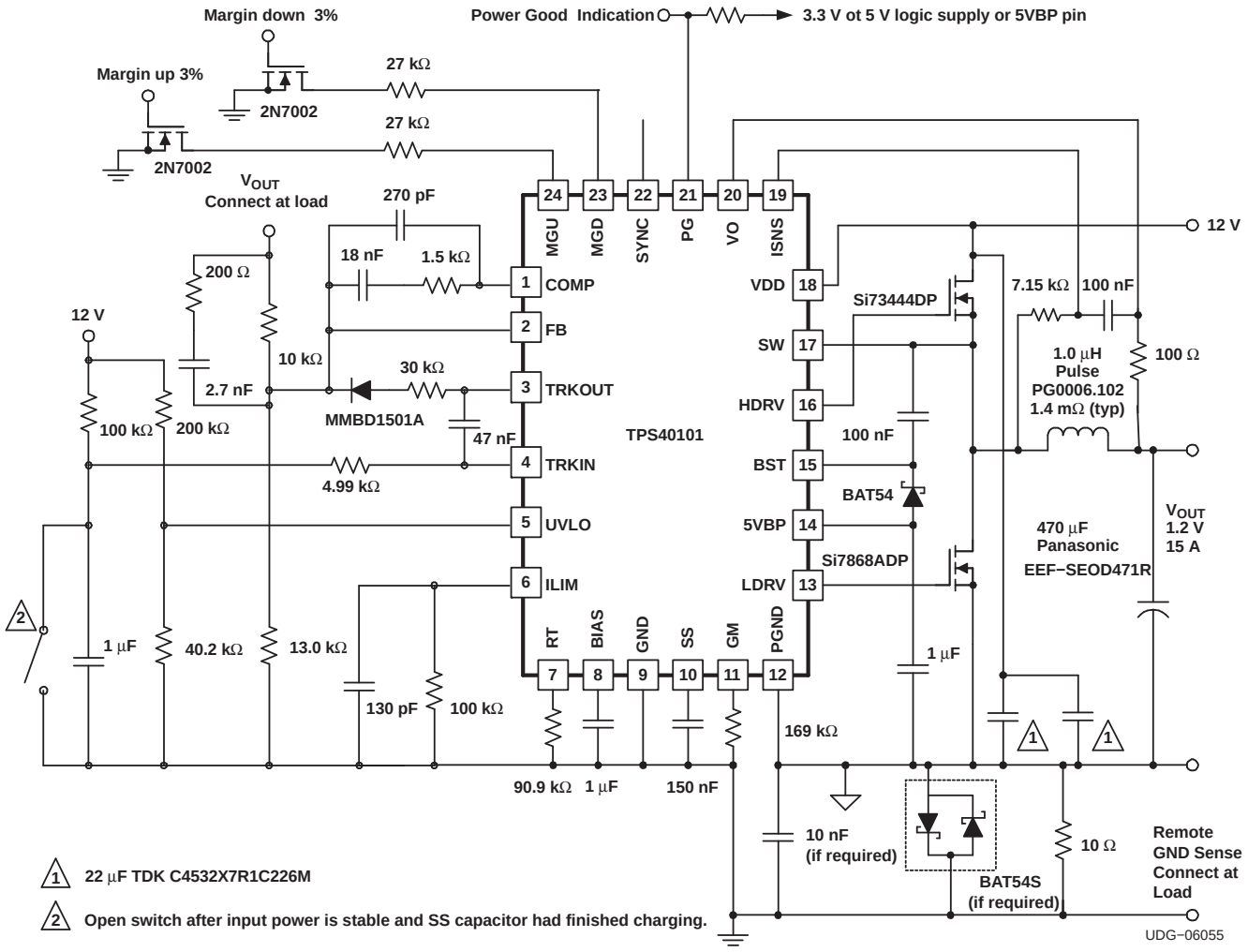


Figure 38. 500-kHz, 12-V to 1.2-V Converter With Tracking Startup Capability and Remote Sensing

ADDITIONAL REFERENCES

Related Parts

The following parts have characteristics similar to the TPS40101 and may be of interest.

Related Parts

DEVICE	DESCRIPTION
TPS40100	Midrange Input Synchronous Controller with Advanced Sequencing and Output Margining
TPS40075	Wide Input Synchronous Controller with Voltage Feed Forward
TPS40190	Low Pin Count Synchronous Buck Controller

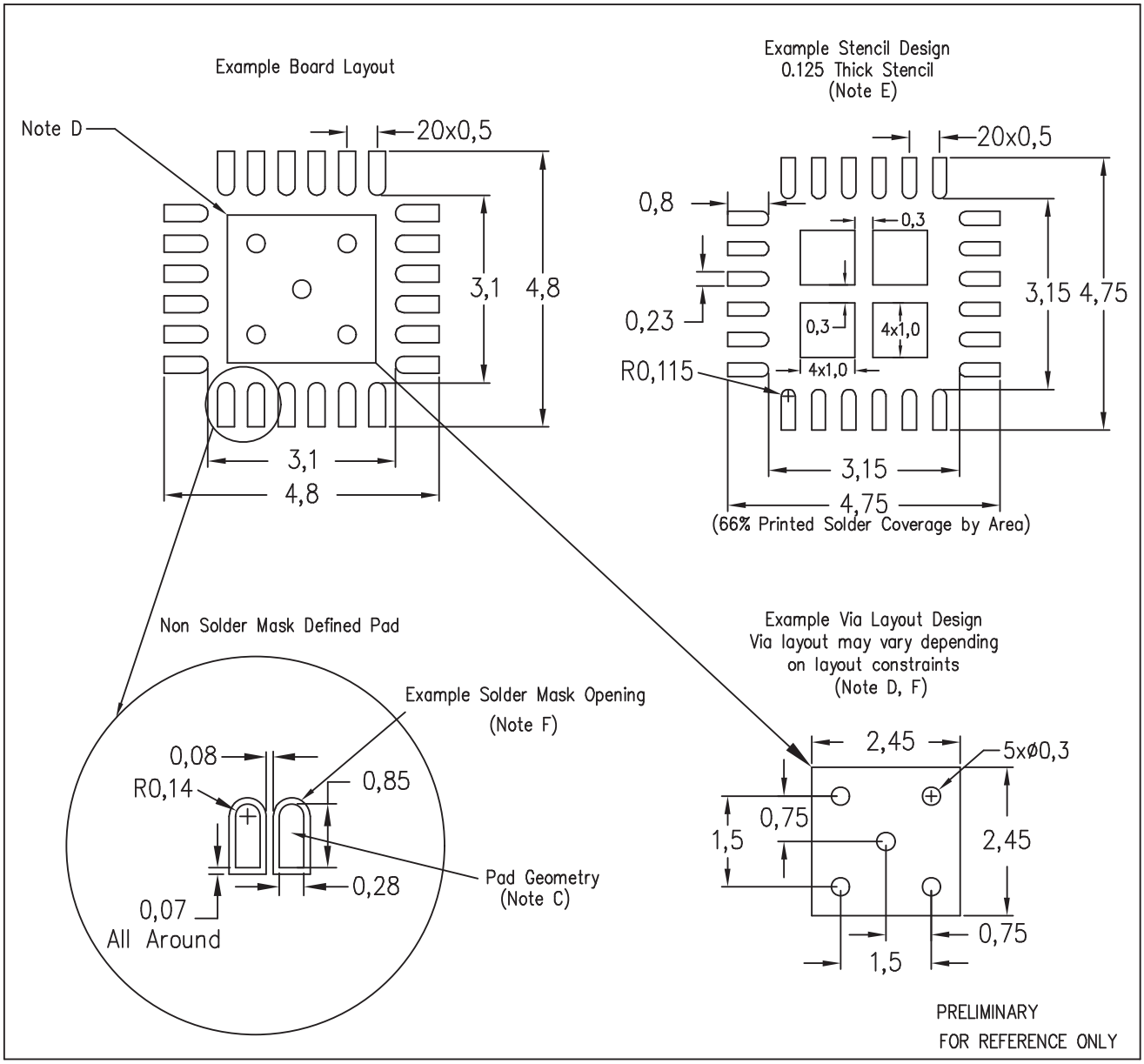
References

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, including design software, may also be found at www.power.ti.com

1. *Under The Hood Of Low Voltage DC/DC Converters*, SEM1500 Topic 5, 2002 Seminar Series
2. *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057, March 1999
3. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
4. *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
5. Additional PowerPAD™ information may be found in Applications Briefs SLMA002 and SLMA004
6. QFN/SON PCB Attachment, Texas Instruments Literature Number SLUA271, June 2002

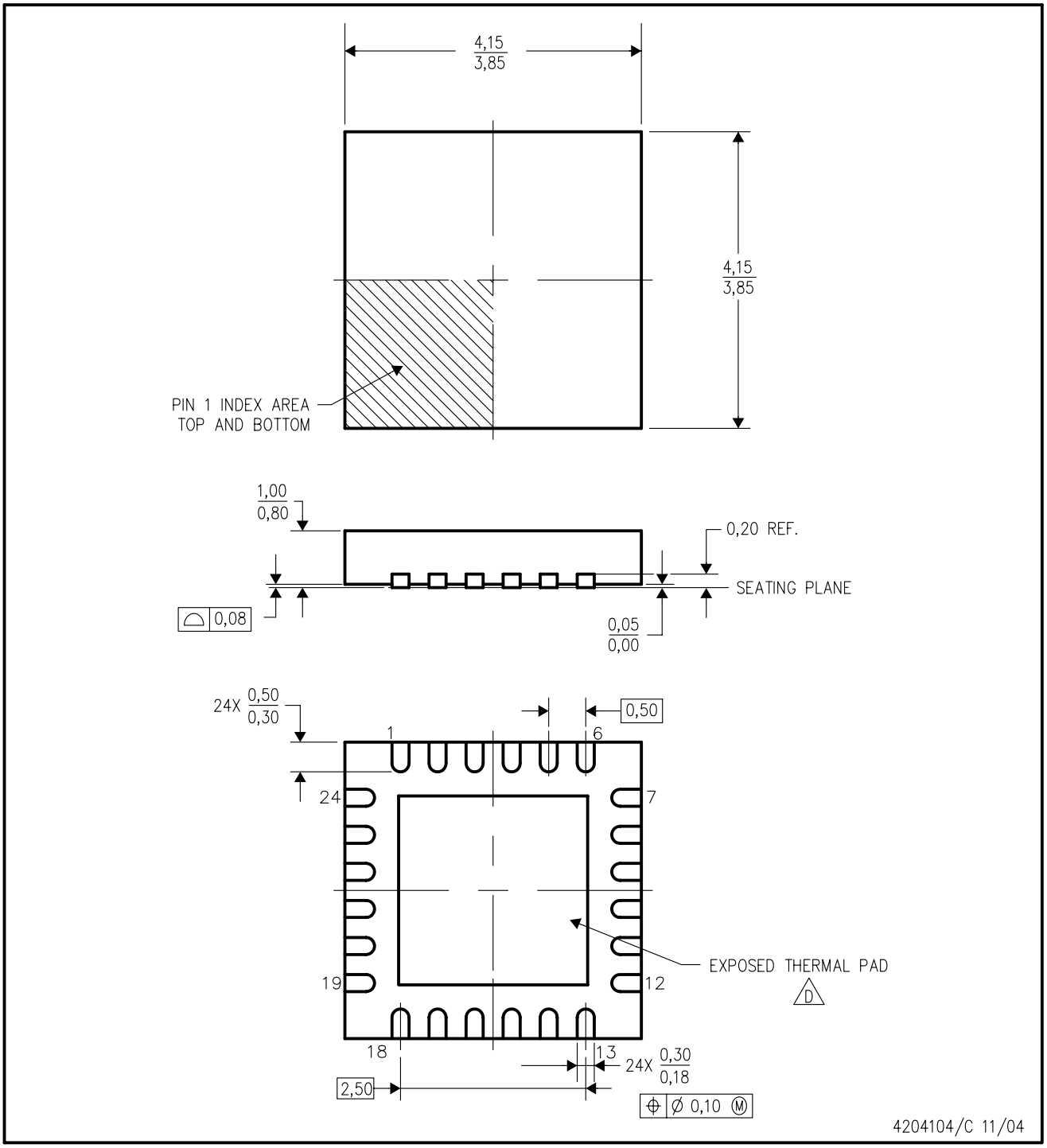
EXAMPLE LAND PATTERN

RGE (S–PQFP–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RGE (S–PQFP–N24) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

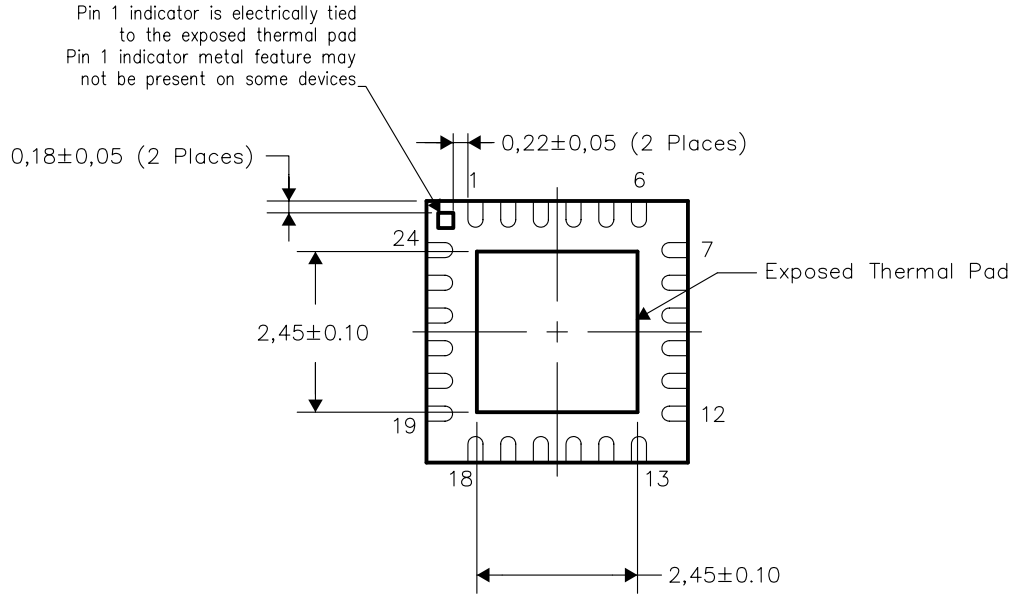
RGE (S–PQFP–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



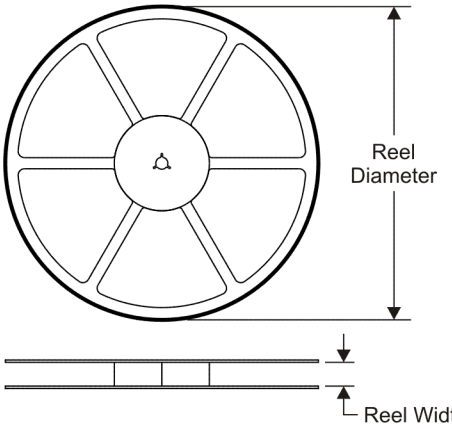
Bottom View

NOTE: All linear dimensions are in millimeters

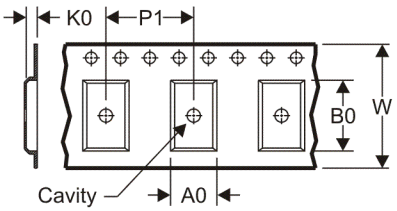
Exposed Thermal Pad Dimensions

TAPE AND REEL INFORMATION

REEL DIMENSIONS

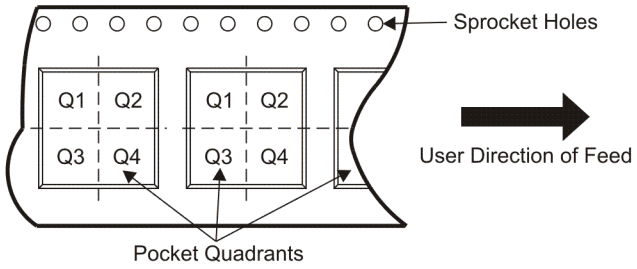


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

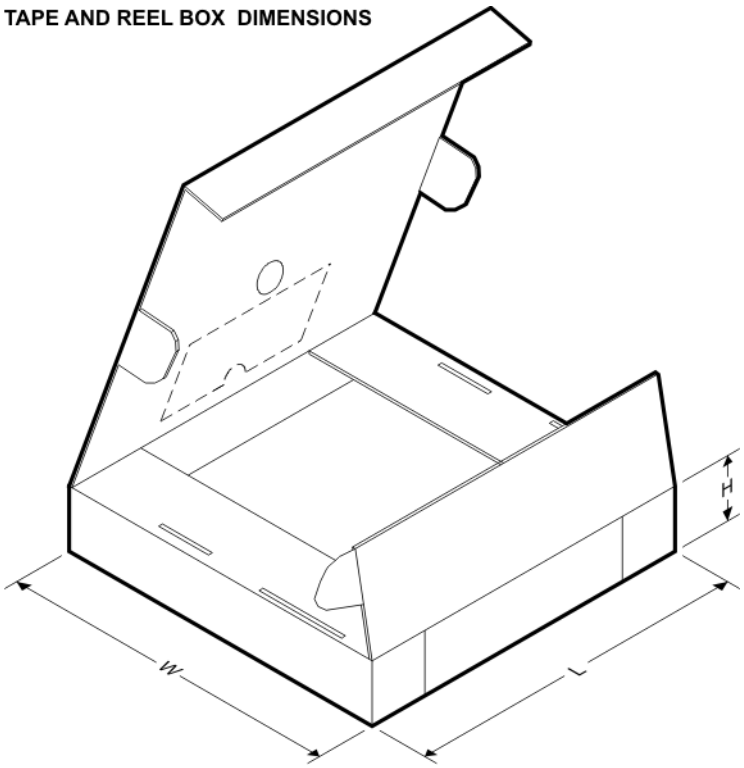
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40101RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS40101RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

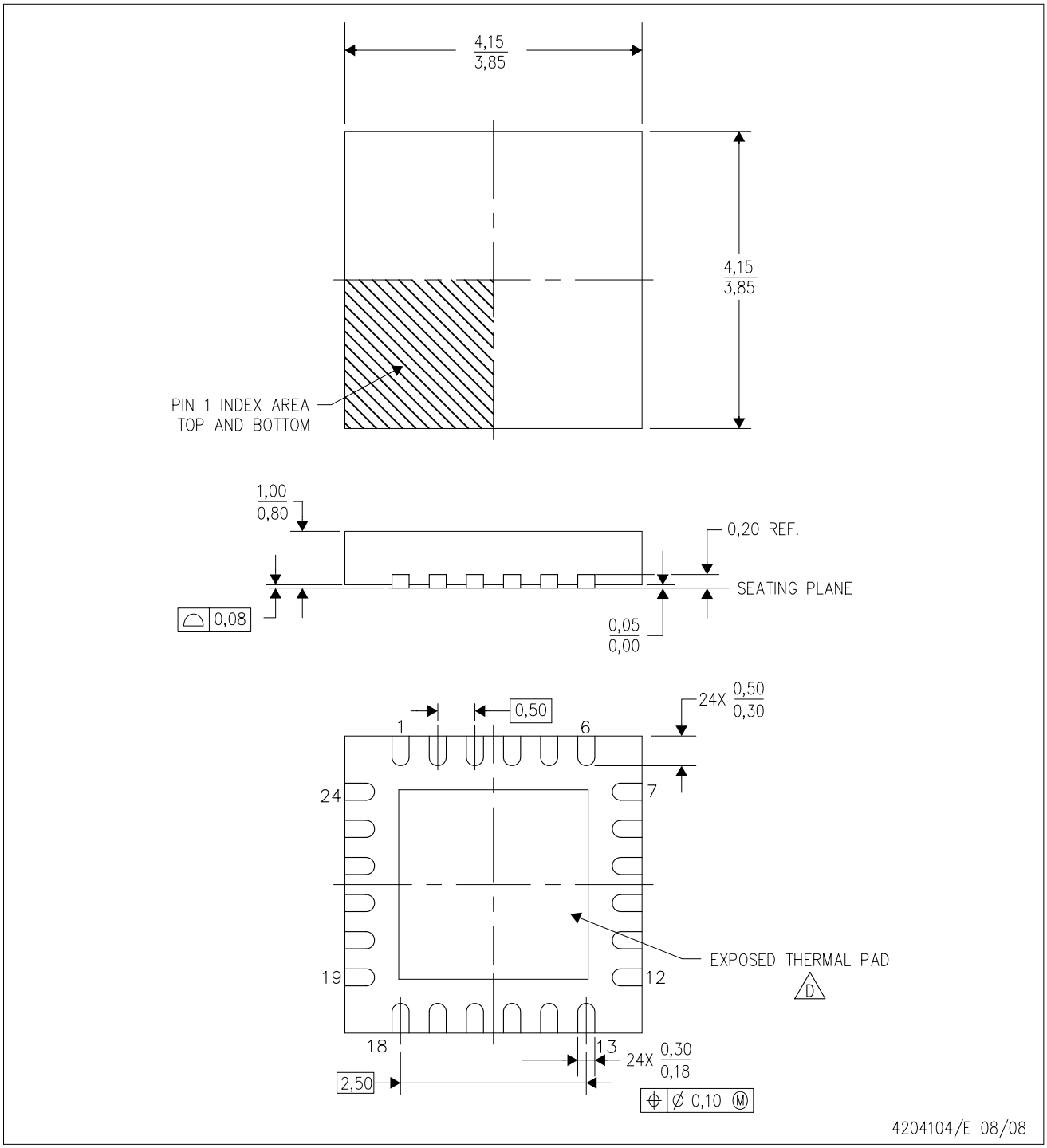
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40101RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
TPS40101RGET	VQFN	RGE	24	250	190.5	212.7	31.8

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

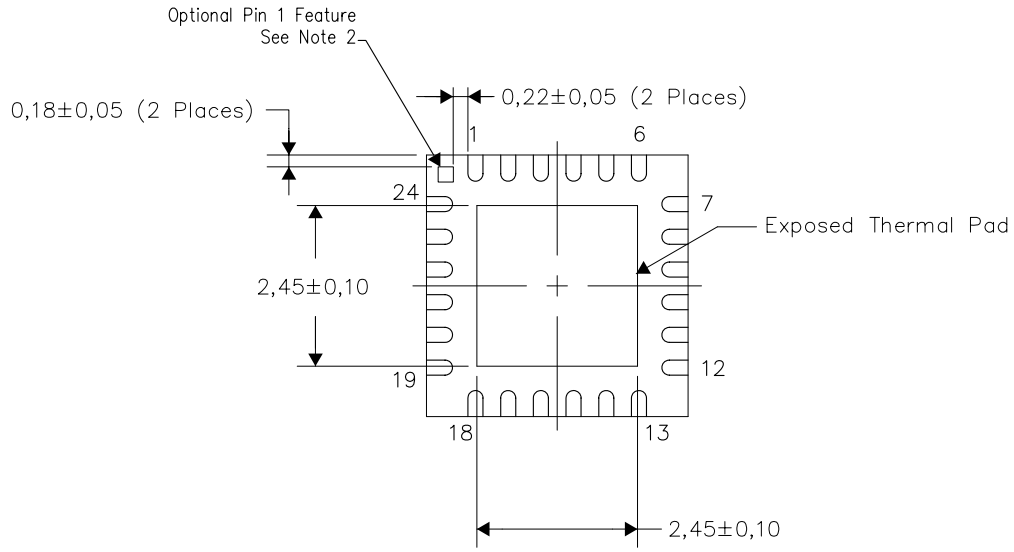
RGE (S–PVQFN–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



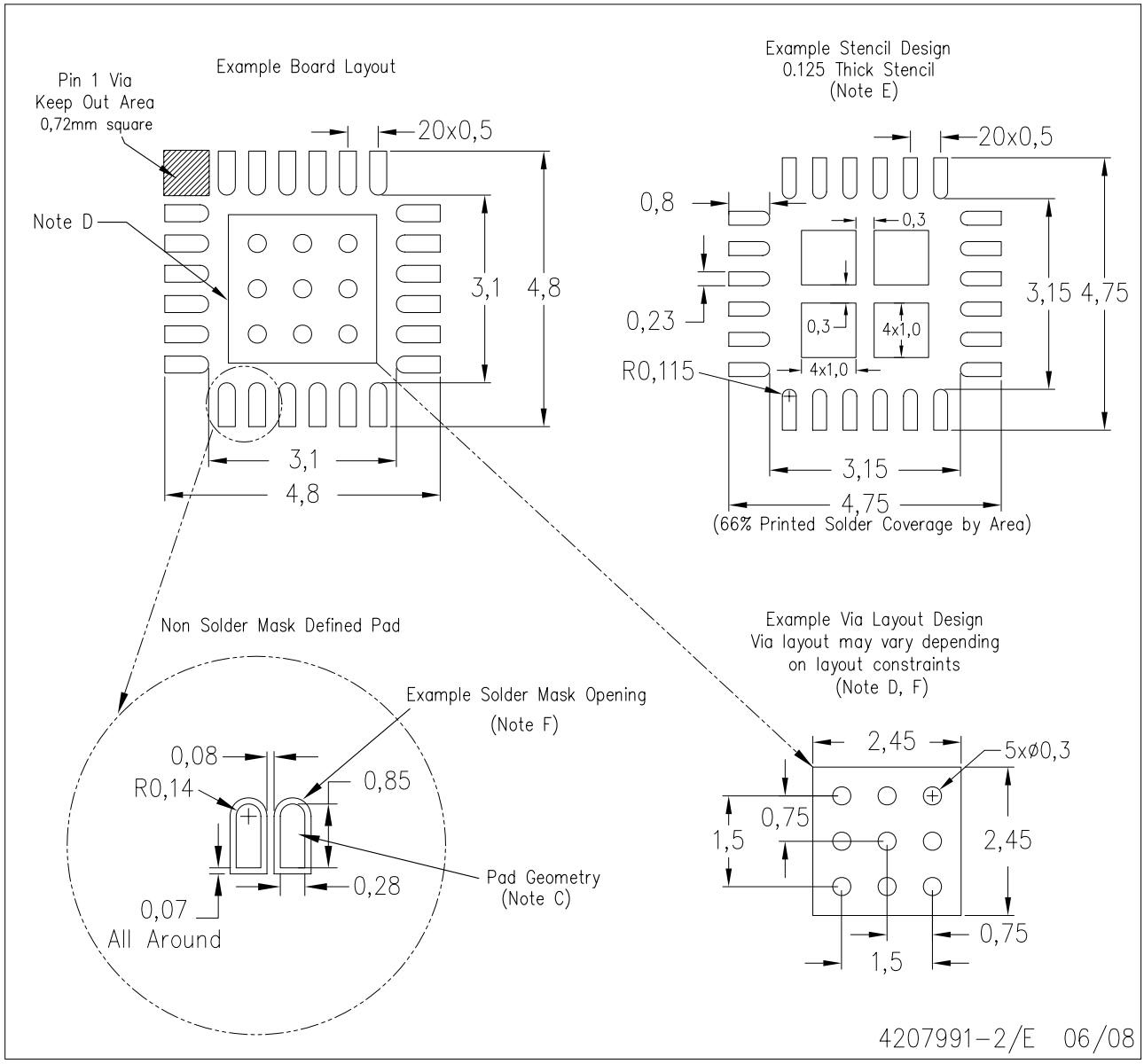
Bottom View

Exposed Thermal Pad Dimensions

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices
   In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S–PVQFN–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265